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Parallel Load Scan Architecture – Impact on Test Application Time

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Abstract
ATPG tool generated vectors are loading into scan chains by serially shifting them, which leads to increase the test application time. This paper proposes new scan architecture to load the test vectors into scan chains in parallel, thereby maximum of test application time can be reduced. Also the proposed architecture supports regular serial scan shifting as well. The ineffective test vectors can be bypassed in the proposed scan structure during the vector generation, thus it will not increase the test data volume. Another major advantage, since all the scan cells in the scan chain are loaded in parallel, it is easy to find the faulty scan cells(s) in the scan chain test.

Keywords
ATPG (Automatic Test Pattern Generate), DFT (Design For Test), LFSR (Linear Feedback Shift Register), SOC (System On Chip).

I. Introduction

Chip manufacturing test contributes a significant portion to the overall cost for the tester time required for test application. Various techniques are proposed for test application time reduction in many articles [1-6]. Test data volume reduction is one of the main errands in the reduction on test time. Due to the larger designs and shrinking technologies in the recent trends, the number of fault models are increasing which accumulate more test data. The increasing test data volume is proportional to the desired coverage, maximum scan chain length and the number of scan chains. An insight on test data volume for SOCs is discussed in [7].

Test compression techniques work by reducing the scan chain lengths and increasing the number of chains by using additional hardware for test data distribution among the scan chains [8]. Several DFT designs use embedded testing logic like LBIST (Logic Built In Self Test) and MBIST (Memory Built In Self Test), involve generate test vectors internally and verify themselves to avoid more external test vectors at the same time thereby reducing the test application time [9-10].

The time taken to complete a single test is proportional to the length of the scan chains, as the test vectors are loading into scan chains in serial. The proposed architecture in this paper evade the serial shifting and load the test vectors into scan chains in parallel, thereby it saves much test application time. The proposed architecture works with random pattern and not by deterministic pattern. The random pattern generation may leads to increase the test data volume, but the proposed architecture can bypass the vectors which are not really effective, thus it will not increase the test data volume.

This paper is structured as follows; the next section discusses the regular scan architectures used in DFT designs. Section three and four addresses the proposed scan architecture with 2-bit and 4-bit LFSR respectively. Section five illustrates how to find the faulty scan cell(s) in scan chain test. Finally the work is concluded in sixth section.

II. Regular Scan Architectures

Full-scan design, Partial-scan design and Random access scan design are the three popular architectures widely used in scan designs. In full-scan design, all storage elements are replaced into scan cells and combinational ATPG is used for test generation [11]. Subsets of storage elements are converted into scan cells and sequential ATPG is used for test generation in partial-scan design [12]. The random-access scan design works with a random addressing mechanism, which is used to provide direct access to read or write any scan cell in random-access scan design [13].

Full-scan design and partial-scan design are also called as serial scan design, as the test patterns are loading/unloading serially through scan chains. The major advantage of serial scan design is its low routing overhead, as the scan data is shifted through adjacent scan cells in the scan chain. Its major disadvantage, the serial shifting operation increases the test application time and the individual scan cells cannot be controlled or observed. Also all the scan cells in the scan chain are switching at same time, which causes excessive test power dissipation, resulting in circuit damage, low reliability, or even test-induced yield loss.

Random access scan design makes each scan cell randomly and uniquely addressable, similar to storage cells in a memory array. Here all scan cells can be accessed individually for control and observe in any order, as they are organized into a two-dimensional array. It uses a row decoder and a column decoder to achieve the random access capability with $\log_2 N$ bit address shift register, where N is the total number of scan cells, is used to specify which scan cell to access. Its major disadvantage, high routing overhead required to setting up the addressing mechanism. In addition, it may increase the test application time if a large number of scan cells have to be updated for each test vector and addressing of scan cells to be consecutively accessed have little overlap.

III. Proposed Scan Architecture

The test application time with the proposed architecture is disproportionate to the scan chain length, as the scan cells are loading test vectors in parallel. Thus the number of scan chains can be minimized in the SOC, thereby the scan pin counts also be reduced. It is guaranteed that the reduction of test application time can be achieved even for the large number of scan chains in the design. The proposed scan architecture is shown in Fig.1.

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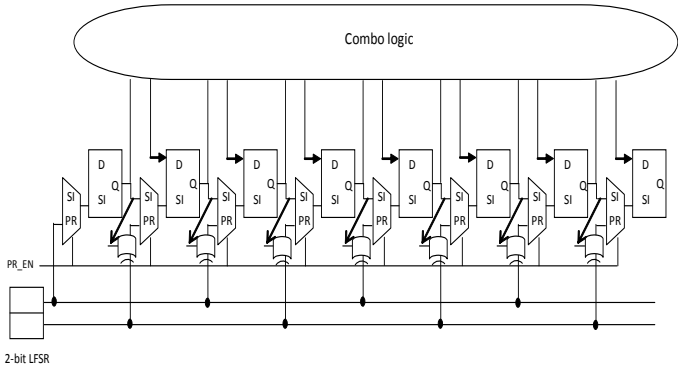

Fig.1: Proposed Scan Architecture with 2-bit LFSR

It includes 2-bit LFSR, Multiplexer and XOR gate. The 2-bit LFSR outputs are connected to all the scan cells alternatively in a scan chain as shown in Fig.1. Each scan cell *Q* output XOR with LFSR value and loading to the next cell when *PR_EN* is 1. The pattern generation flow is shown in Fig.2.

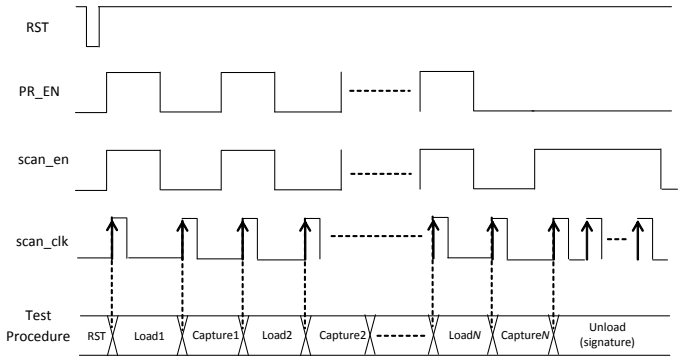

Fig.2: The Pattern Generation Flow

The steps in pattern generation flow as follows;
1. Reset all the scan cells (assume active low reset)

2. Load scan chains
- *PR_EN*=1, *scan_en*=1, load LFSR seed with 2'b11 and apply one pulse in shift cycle. Now all the scan cells getting loaded with XOR-ed values of LFSR and scan cells previous state.

3. Apply capture pulse
- *PR_EN*=0, *scan_en*=0, apply one pulse in capture cycle for stuck-at (two pulses for transition). Now all the scan cells capture the response of combinational logic.

4. Apply another capture pulse (optional)
- The new captured values from step3 also can be considered as one of the pattern. So apply another capture pulse and find the test coverage for this pattern.

5. Repeat step2 and step4 with different LFSR values until it get desired coverage.

6. Unload scan chains
- Once the test coverage is reached to the desired number, make *PR_EN*=0, *scan_en*=1 and pulse *scan_clk* to the maximum of scan chain length.

7. Bypass ineffective pattern
- If the current pattern is not effective, then retain the previous captured values in the scan chain and generate new pattern until get effective pattern by changing LFSR values. Thus the ineffective patterns are bypassed.

The bypassing flow is shown in Fig.3. Assumed pattern2 is ineffective and bypassing the same. While bypassing pattern2, the scan chain retains the pattern1 captured values.

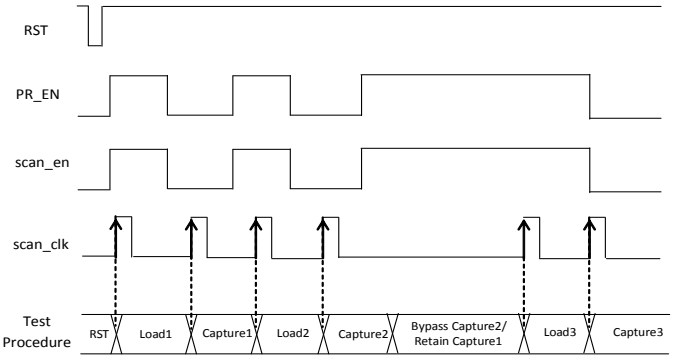

Fig.3: The Pattern Generation Flow

These all the steps to be performed during ATPG and preserve only effective patterns for the production delivery.

IV. Proposed Scan Architecture with 4-bit LFSR

There are maximum of 1+4 different patterns can be verified with the 2-bit LFSR for each load procedure. i.e., captured value + captured value XOR-ed with LFSR values of 00,01,10,11. More patterns can be generated by increasing the LFSR bit size, thus chances of getting effective patterns are high. The proposed scan architecture with 4-bit LFSR is shown in Fig.4.

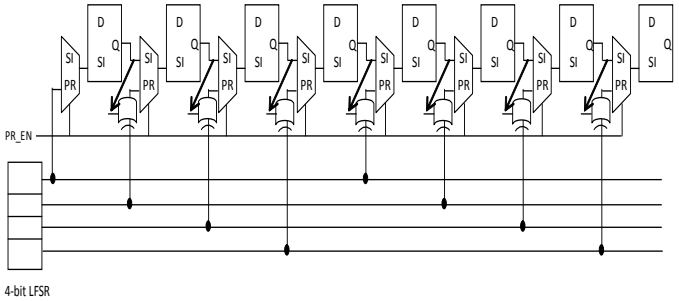

Fig.4: Proposed Scan Architecture with 4-bit LFSR

The 4-bit LFSR outputs are connected alternatively as shown in Fig.4. In this case, 1+16 different patterns can be generated. i.e., captured value + captured value XOR-ed with LFSR values of 0000 to 1111, thereby chances of getting effective patterns are more, but high routing overhead. If the expected test coverage number is not achieved by the proposed parallel scan load test procedure, the remaining coverage can be achieved with the regular scan test procedure (serial load/unload), since the proposed structure work as regular scan structure as well, when *PR_EN*=0.

V. Find Faulty Scan Cell(s) in the Scan Chain Test

Let's assume a 10-bit scan chain and 5th bit position scan cell *Q* output is affected by Stuck-at-0 (SA-0) fault. In the regular serial load scan chain test approach, 6th to 10th bit cells are getting loaded with '0' due to the SA-0 fault in *Q* to *SI*(scan input) path of 5th to

6th bit cell. To find this faulty cell, the 6th bit cell should be loaded with '1', but it is not possible in serial shifting. When shifting out scan chain, the *SO*(scan output) gives '0000000000'. Load '1' to 6th bit cell can be done through functional path during capture, but it is not guaranteed.

It is possible with the proposed scan architecture, as the scan cells are getting loaded in parallel. After reset all the scan cells, the LFSR with '11' makes the scan cells to load '1'. When shifting out the scan chain serially, the *SO* gives '000001111'. So the faulty cell can be found easily.

VI. Conclusion

The major drawback of the proposed scan architecture is routing congestion and area overhead due to additional Multiplexer with XOR for each scan cell and LFSR. This area overhead is negligible when compare to the total area of modern SOCs. In the regular scan architecture, the *scan_en* pin is routed throughout the chip. In the proposed architecture, additionally *PR_EN* pin and LFSR outputs are routed along with the *scan_en* pin. So the routing effort is not much critical. Another major advantage as discussed in previous section, since all the scan cells flops in the scan chain are loaded in parallel, it is easy to find the faulty flop(s) in the scan chain test. Thus, by considering outcome of much reduction in the test application time and increasing test quality with the proposed architecture, the area overhead and routing congestion can be negotiated.

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Author's Profile

Ramkumar Balasubramanian working in DFT (Design For Testability) domain in Altran India Technologies, Bangalore, India. He received Ph.D degree from VIT University, Vellore in 2014. He completed Master of Engineering in VLSI design, 2006 and Bachelor of Engineering in Electronics & Communication, 2004.