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Logic Design for Single On-Chip Test Clock Generation for *N* Clock Domain - Impact on SOC Area and Test Quality

Ramkumar Balasubramanian
Altran Technologies, Bangalore, India

Abstract
This paper proposes a design technique for single On-Chip test Clock (OCC) generation logic to use multiple clock domain, to reduce significant area overhead of using multiple OCC. It reduces test vector count and increases test quality that is discussed with ATPG results. The area comparison data reported in this work shows that almost 50% to 70% area overhead reduced by the proposed OCC than using regular OCC for N clock domains. The proposed design techniques are easy to implement with any kind of existing OCC structure.

Keywords
DFT-Design For Testability, OCC, SOC-System On Chip, Area Reduction, ATPG (Automatic Test Pattern Generation)

I. Introduction

Structural fault testing of digital integrated circuits is a major tradition in the semiconductor industry. Adding testability features in the hardware design, which makes easier to perform manufacturing tests for the designed hardware. Adding the basic testability feature starts with creating scan chains in the design to capture the faults [1-2]. The combination of scan test with Automatic test pattern generation (ATPG) for transition and stuck-at test have been the industry standard for many years [3-5].
To perform transition test, *OCC* is a core logic used in the design to generate launch and capture pulse. There are different algorithms like Launch-On-Shift (LOS) and Launch-On-Capture (LOC) performed using *OCC* for transition test [6-8]. Modern SOC's contain many blocks with multiple clock domains, and to target transition test for each clock domain they requires one *OCC* per clock domain. This makes additional area overhead in the actual SOC design. Let's consider, a SOC contain 20 blocks and each block has 5 different clock domains. If the *OCC* implemented at each block level, it requires 100 *OCC* to perform transition test excluding top level test for SOC. The area consumption for 100 *OCC* is huge in the SOC. This paper proposes an *OCC* structure which can be used for *N* different clock domains, which means one *OCC* for multiple clock domains. In the above example (20 blocks SOC) with the proposed *OCC*, there are only 20 *OCC*'s required to perform transition test by having one *OCC* per block. So it saves area overhead of 80 *OCC*'s in the SOC. Clock shaper is used in many designs to generate test clock for multiple clock domains. This paper proposes the design technique for how to use the single *OCC* structure for multiple clock domains with simple modifications.
Test clock staggering approach reduces the test pattern count which increases the test quality [9-11]. The proposed *OCC* generates the test clock in staggered manner for transition and stuck-at test, which are discussed in the upcoming sections.
The paper is structured as follows; the next section discusses the logic design of *OCC* used for per clock domain and the area consumption. Section three addresses implementation details of the *OCC* for *N* clock domain and area comparison. Three pulse generation *OCC* structure is given in section four. The fifth section discusses the transition test and stuck-at test generation with ATPG results. Finally, the work is concluded in sixth section.

II. Logic Design of OCC Structure for Single Clock Domain

The basic *OCC* design was discussed by M.Beck et al in 2005 with ATPG experimental results [12]. Fig.1 shows the regular *OCC* structure, which is slightly modified from the M.Beck's design. The behaviour of this *OCC* is shown in Fig.2 (a) and Fig.2 (b) for transition test and stuck-at test respectively. In many cases, the *OCC* is not used for stuck-at test. In this work, the *OCC* is designed to support both Transition Fault Test (TFT=1) and stuck-at fault test (TFT=0).
It consists of n-bit shift register, which decides the delay between *scan_en* asserts low to launch pulse of transition test (capture pulse in stuck-at test). During the *scan_en* high, the *clk_out* Mux is connecting *scan_clk* to the *clk_out*. When *scan_en* asserts low, the shift register starts shifting '1' and *pll_clk_en* makes '1' to the Clock Gater (CG) to allow single pulse or double pulse from PLL depending on TFT.

Since the *OCC* structure is smaller, the area required to implement *OCC* is manually calculated in terms of number of instances that are listed in Table 1. The shift-register size determines the delay between each clock domain capture pulse. In this paper, 6-bit shift-register is used for experiments. The total area count of one *OCC* is negligible when compare to entire SOC area. The actual problem starts, when this negligible area increased to *N* times, where *N* is number of clock domain. The next section illustrates the same *OCC* structure is slightly modified and used for *N* clock domain to reduce the area overhead of *N-OCC*'s

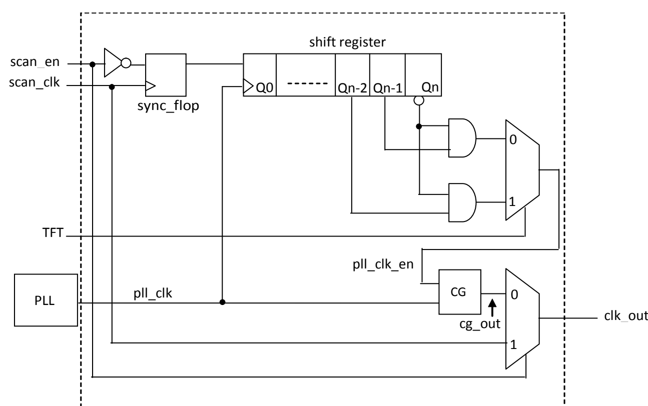

Fig. 1: Regular OCC structure

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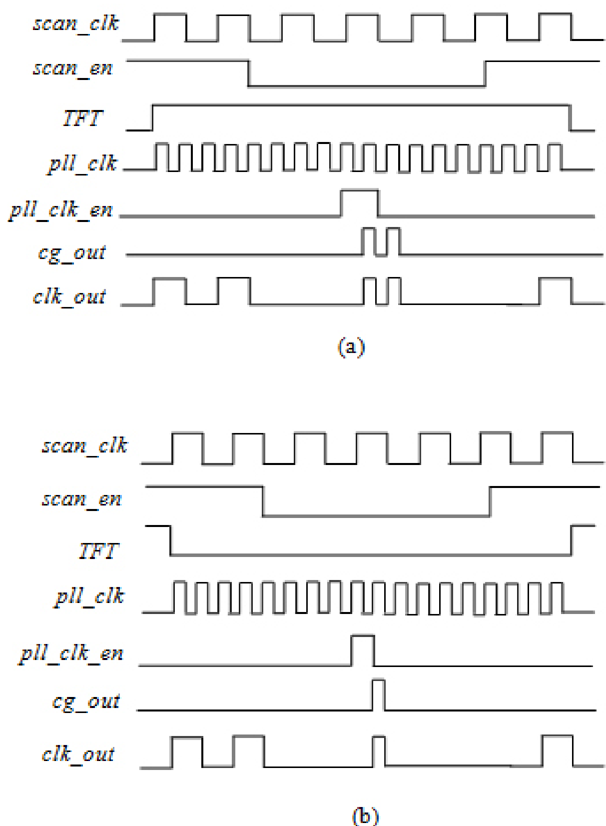

Fig. 2: Regular OCC behaviour - (a) For Transition Test, (b) For Stuck-at Test

Table 1 : Area Count for Regular OCC

Instance name	Number of Instance's
Inverter	1
Shift-register flops	6
Sync-flop	1
AND	2
2:1 Mux	2
CG	1
Total	**13**

III. Logic Design of Proposed OCC Structure for *N* Clock Domains

The regular OCC structure is slightly modified in the shift-register by making feedback the output to input. There is additional logic of Counter, multiplexer (Mux) and de-multiplexer (Demux) added in the design. The proposed OCC structure for 4-clock domain is shown in Fig.3. The behaviour of this OCC is shown in Fig.4 for transition test. The output clocks (*clk_out1* to *clk_out4*) are pulsed in staggered manner between each PLL clock domain (*pll_clk1* to *pll_clk4*).

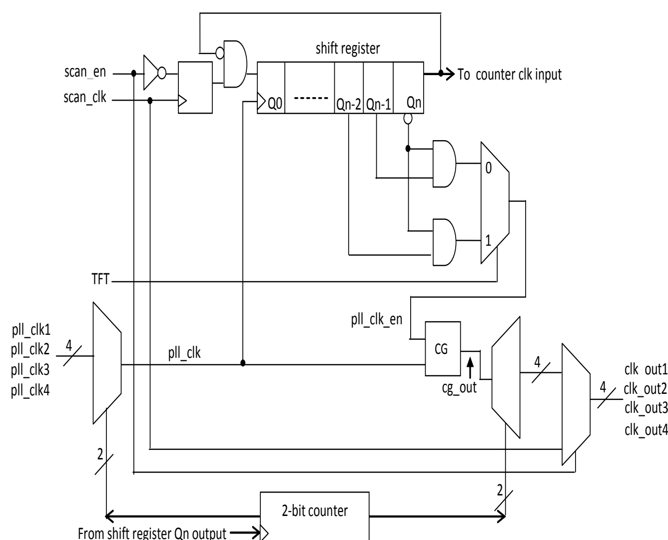

Fig. 3: Proposed *OCC* Structure for 4 Clock Domains

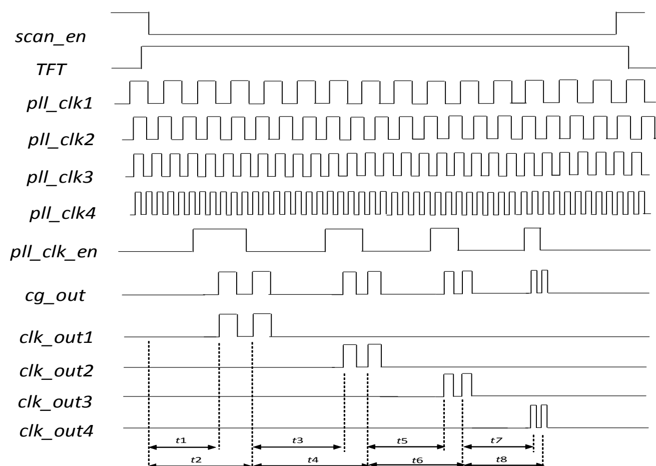

Fig. 4: Proposed *OCC* behaviour for 4 Clock Domain

The detailed behaviour of the proposed *OCC* is illustrated in below steps;

1. When *scan_en* is high, the *clk_out* Mux is connecting *scan_clk* to *clk_out*.
2. When *scan_en* is low, the *pll_clk*1 is selected by default initial value of counter (00) and the shift-register starts shifting '1' which is controlled by *pll_clk*1. For transition test, the launch pulse for this *pll_clk*1 comes when the shift-register shifting '1' at *Qn*-2 bit position and capture pulse comes at *Qn*-1 bit position. The delay t1 between *scan_en* low to the launch pulse is (*tQn*-2)**pll_clk*1 and for capture pulse delay t2 is (*tQn*-1)**pll_clk*1; where, *tQn*-2 is the time delay for shifting '1' from *Q*0 to *Qn*-2 bit position at *pll_clk*1 frequency and *tQn*-1 is (*tQn*-2)+1.
3. The *Q*0 gets inverted value from *Qn* while *scan_en* remains low, and the shift-register starts shifting its new value '0' which is controlled by *pll_clk*2. The counter increases when the shift-register *Qn* toggles 0 to 1. For transition test, the launch pulse for this *pll_clk*2 comes only again the shift-register is shifting '1' at *Qn*-2 bit position and capture pulse comes when '1' at *Qn*-1 bit position. The delay between *pll_clk*1 capture pulse and *pll_clk*2 launch pulse is ((*tQn*+(*Qn*-2))**pll_clk*2), where, *tQn* is time delay for shifting '0' to the

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entire shift-register and *Qn*-2 is time delay for shifting '1' to *Qn*-2 bit position.

4. The behavior of step3 follows for *pll_clk*3 and *pll_clk*4.
5. Delay timing for all the *pll_clk*'s in transition test can be defined as follows,

- *scan_en* low to the launch pulse of *pll_clk*1 (t1) = (*tQn*-2)**pll_clk*1
- *scan_en* low to the capture pulse of *pll_clk*1 (t2) = (*tQn*-1)**pll_clk*1
- *pll_clk*1 capture pulse to *pll_clk*2 launch pulse (t3) = (*tQn*+(*Qn*-2))**pll_clk*2
- *pll_clk*1 capture pulse to *pll_clk*2 capture pulse (t4) = (*tQn*+(*Qn*-1))**pll_clk*2
- *pll_clk*2 capture pulse to *pll_clk*3 launch pulse (t5) = (*tQn*+(*Qn*-2))**pll_clk*3
- *pll_clk*2 capture pulse to *pll_clk*3 capture pulse (t6) = (*tQn*+(*Qn*-1))**pll_clk*3
- *pll_clk*3 capture pulse to *pll_clk*4 launch pulse (t7) = (*tQn*+(*Qn*-2))**pll_clk*4
- *pll_clk*3 capture pulse to *pll_clk*4 capture pulse (t8) = (*tQn*+(*Qn*-1))**pll_clk*4

6. The capture pulse behavior of the transition test is similar for stuck-at.

The area detail of the proposed *OCC* structure is shown in Table 2. There are 2 Inverters used in the design, where in one at *scan_en* path and another one at shift-register feedback path.

Table 2 : Area Count of Proposed OCC for 4 Clock Domain

Instance name	Number of Instances
Inverter	2
Shift-register flops	6
Sync-flop	1
AND	3
2:1 Mux (for *pll_clk_en*)	1
CG	1
2:1 Mux (for *clk_out*1 to *clk_out*4)	4
4:1 Mux interms of 2:1 Mux (for *pll_clk*1 to *pll_clk*4)	3
1:4 DeMux interms of 1:2 Demux	3
2-bit counter flops	2
Total	**26**

Area comparison between the regular *OCC* and proposed *OCC* for 4 to 32 clock domain is reported in Table 3. The comparison graph is shown in Fig.5. An equation derived to determine the area required for *N*-clock domain as follows,

Regular *OCC* = *N* * 13
Proposed *OCC* = 14 + ((*N*-1)*2) + *N* + log2n

Where,

- *N* = Number of clock domain
- 13= Area of regular *OCC* for one clock domain
- 14= Number of instances in the proposed *OCC* excluding 2:1 Mux for *clk_out*, 2:1 Mux for *pll_clk*, 1:2 Demux and counter flops. (For example, In Table.2 excluding last 4 instances)
- *N*-1*(2) = Number of 2:1 Mux for *pll_clk* + 1:2 Demux for *clk_out*
- $\log_2 N$ = Number of flops in counter

Tabel 3 : Area Comparison between Regular OCC and Proposed OCC for 4 to 32 Clock Domains

Number of Clock Domain	Area for Regular *OCC*	Area for Proposed *OCC*	% of area reduction in Proposed *OCC*
4	52	26	50
8	104	39	63
16	208	64	69
32	416	113	73

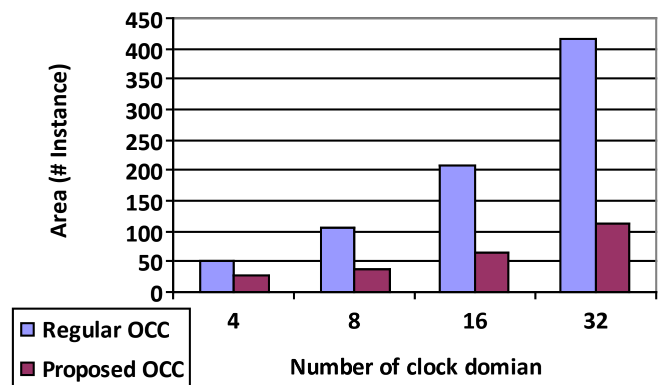

Fig. 5: Performance of Proposed *OCC* than Regular *OCC* for 4 to 32 Clock Domains

The comparison results are clearly shows that the area of the proposed *OCC* structure is reduced 50%, 63%, 69% and 73% than regular *OCC* for 4,8,16 and 32 clock domains respectively.

IV. Three Pulse Generation for Transition Test

This paper proposed a design idea of using single *OCC* for multiple clock domains. This logic can be modified further as required. For example, some designs are required more than one launch pulse in transition test, based on their sequential depth. It can be done by using a configurable register in the design as shown in Fig.6. This configurable register is pre-loaded with '1' to select three pulses for *pll_clk*3 domain. The behavior of this *OCC* is shown in Fig.7.

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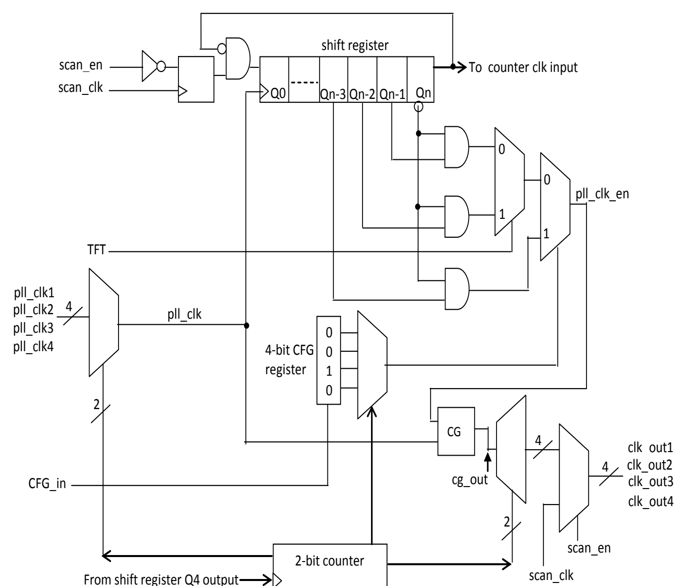

Fig. 6: Proposed *OCC* Structure for 4 Clock Domain and 3 capture pulse for *pll_clk*3

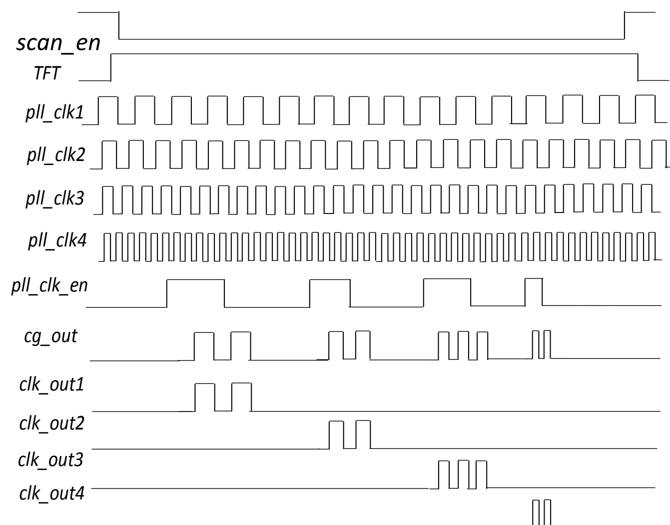

Fig. 7: Proposed *OCC* behaviour for 4 Clock Domain and 3 capture pulse for *pll_clk*3

V. ATPG Experiments for Transition and Stuck-at Test

The proposed *OCC* is designed for 6 clock domain and used in one of the 6 different clock domain netlist to perform transition & stuck-at test by having different clock frequency for *pll_clk*1 to *pll_clk*6. The netlist contains ~40,000 scan flops which are connected in 176 balanced internal scan chains with the maximum chain length of 231, based on EDT (Embedded Deterministic Test) architecture. There are four experiments has been done to determine the impact of proposed *OCC* on fault coverage and pattern count. The experimental results are listed in Table 4.

Exp1: Transition test - using a Regular OCC per clock domain:
It used one regular *OCC* per clock domain capture as shown in Fig.1 (with TFT=1). Here each domain clock pulsed at different capture cycle. i.e., it targets one clock domain faults per capture cycle.
Exp2: Transition test - using proposed OCC:
This exp used the proposed *OCC* for all the clock domains as shown in Fig.3 (with TFT=1). Here each domain clock pulsed at same capture cycle in staggered manner as shown in Fig.4.
Exp3: Stuck-at test - using a regular OCC per clock domain:
In regular approach, a common external scan clock used for all the clock domains for stuck-at test. Since this paper demonstrates *OCC* for single pulse generation, this exp uses one regular *OCC* per clock domain capture. This exp is similar to exp1 with TFT=0.
Exp4: Stuck-at test - using proposed OCC:
This exp is similar to exp2 with TFT=0.

Table 4 : Experimental Results

Exp	Test Coverage (%)	Pattern Count
Exp1	93.89	5449
Exp2	93.89	5066
Exp3	95.37	2233
Exp4	95.37	1928

The test coverage is same for transition faults using regular and proposed *OCC*, but the pattern count is reduced 383 by using the proposed *OCC*. For stuck-at test also, the test coverage is same in both cases and pattern count is reduced 305 with the proposed *OCC*. These experimental results are clearly shows that the proposed *OCC* is not affecting the actual test coverage and saves the pattern count. The aim of these experiments is to show the proposed *OCC* is not affecting the actual coverage of using the regular *OCC*, hence the author is not analyzed the reaming untested faults in above experiments. Therefore the proposed *OCC* increases the test quality by reducing the pattern count and preserving the actual test coverage.

VI. Conclusion

Modern structural testing approaches target each clock domain faults sequentially (staggered) to avoid more switching power consumption. Since all the clock domain faults are not targeted at same time, it is really not required to run multiple *OCC*'s in parallel. A simple modification applied in the regular *OCC* structure proposed in this paper saves significant area overhead of using multiple *OCC* in the SOC, which is proved in the area comparison results in section 3. This modification can be applied to any kind of existing *OCC* structure to use for multiple clock domains. The ATPG result shows that there is no affect on actual test coverage and saves pattern count with the proposed *OCC*. Therefore the proposed *OCC* structure is simple and efficient to implement in SOC.

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Author Profile

Ramkumar Balasubramanian working in DFT (Design For Testability) domain in Altran India Technologies, Bangalore, India. He received Ph.D degree from VIT University, Vellore in 2014. He completed Master of Engineering in VLSI design, 2006 and Bachelor of Engineering in Electronics & Communication, 2004.

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