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Low-Cost FIR Filter Designs Based on Faithfully Rounded Truncated Multiple Constant Multiplication/Accumulation

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Abstract
Digital signal processing is an area of science and engineering that has developed rapidly over the past 30 years. This rapid development is a result of the significant advances in digital computer technology and integrated -circuit fabrication. The digital computers and associated digital hardware of three decades ago were relatively large and expensive and, as a con sequence, their use was limited to general-purpose non-real-time (off-line) scientific computations and business applications[1].
Finite impulse response (FIR) digital filter is one of the fundamental components in many digital signal processing (DSP) and communication systems. The Design of Direct form FIR filter is based on Truncated Multiplication, in place of multiplier less and memory based multiplication[2].
In this wok to increase the speed and to reduce the complexity of FIR filter we implemented by using Vedic multiplier. Vedic multipliers are faster multipliers as compare to the other multiplication techniques. As extension to this we also designed transposed form FIR filter. The complete project will be implemented in Verilog and will be tested on Xilinx FPGAs.

Keywords
FIR, Verilog, FPGA, DSP,vedic multiplier.

I. Introduction

Finite impulse response (FIR) digital filter is one of the fundamental components in many and communication systems. It is also widely used in many portable applications with limited area and power budget. A general FIR filter of order *M* can be expressed as,

$$y[n] = \sum_{i=0}^{M-1} a_i x[n-i] \quad (1)$$

In case of linear phase, the coefficients are either symmetric or anti-symmetric with *ai* = *aM*−*i* or *ai* = −*aM*−*i*. There are two basic FIR structures, direct form and transposed form, as shown in Figure 1 for a linear-phase even-order FIR filter. In the direct form in Figure 1(a), the multiple constant multiplication (MCM)/accumulation (MCMA) module performs the concurrent multiplications of individual delayed signals and respective filter coefficients, followed by accumulation of all the products. Thus, the operands of the multipliers in MCMA are delayed input signals *x*[*n* − *i*] and coefficients *ai*. In the transposed form in Figure 1(b), the operands of the multipliers in theMCM module are the current input signal *x*[*n*] and coefficients. The results of individual constant multiplications go through structure adders (SAs) and delay elements.
In the past decades, there are many papers on the designs and implementations of low-cost or high-speed FIR filters. In order to avoid costly multipliers, most prior hardware implementations of digital FIR filters can be divided into two categories: multiplierless based and memory based. Multiplierless-based designs realize MCM with shift-andadd operations and share the common suboperations using canonical signed digit (CSD) recoding and common subexpression elimination (CSE) to minimize the added cost of MCM[3].

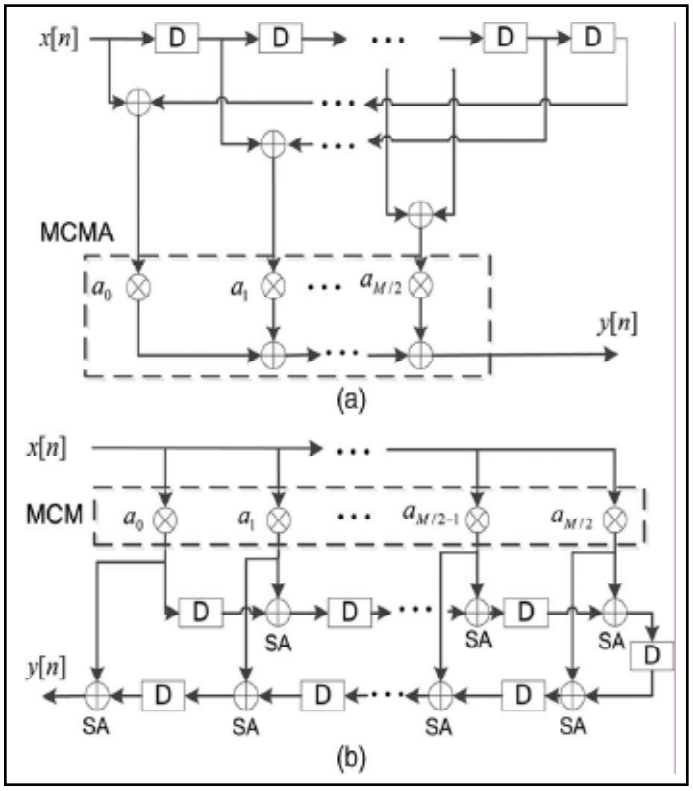

Fig. 1 : Structures of linear-phase even-order FIR filters: (a) Direct form and (b) transposed form.

II. Existing FIR Implementations

A. Design of FIR filters

Finite-impulse response (FIR) digital filter is widely used as a basic tool in various signal processing and image processing applications. The order of an FIR filter primarily determines the width of the transition-band, such that the higher the filter order, the sharper is the transition between a pass-band and adjacent stop-band. Many applications in digital communication (channel equalization, frequency channelization), speech processing (adaptive noise cancelation), seismic signal processing (noise elimination), and several other areas of signal processing require

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filter output increases linearly with the filter order, real-time implementation of these filters of large orders is a challenging task. Several attempts have, therefore, been made and continued to develop low-complexity dedicated VLSI systems for these filters[4].

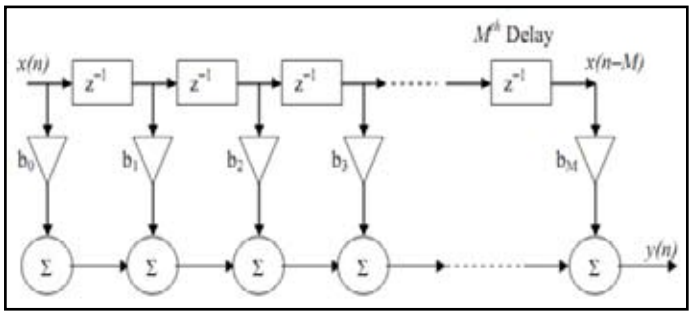

Fig. 2 : FIR filter

In this section we describe several methods for designing FIR filters. Our treatment is focused on the important class o f linear-phase F IR filters. Symmetric and Anti symmetric FIR Filters An FIR filter of length *M* with input *x (n)* and output *y(n)* is described by the difference equation.

$$y(n) = b_0x(n) + b_1x(n-1) + \cdots + b_{M-1}x(n-M+1) = \sum_{k=0}^{M-1} b_kx(n-k) \quad (2)$$

Where {bk} is the set o f filter coefficients. Alternatively, w e can express the output sequence as the convolution o f the unit sample response *h(n)* o f the system with the input signal. Thus we have

$$y(n) = \sum_{k=0}^{M-1} h(k)x(n-k) \quad (3)$$

Where the lower and upper limits on the convolution sum reflect the causality andfinite-duration characteristics o f the filter. Clearly, (8.2.1) and (8.2.2) are identical in form and hence it follows that
bk = *h(k), k* = 0 , 1 , . . . , *M* ~ 1 .

B. FIR filter design using LUT multiplier

Finite Impulse Response (FIR) digital filter is widely used as a basic tool in various signal processing and image processing applications. The order of an FIR filter primarily determines the width of the transition-band, such that the higher the filter order, the sharper is the transition between a pass-band and adjacent stop-band. Many applications in digital communication (channel equalization, frequency channelization), speech processing (adaptive noise cancelation), seismic signal processing (noise elimination), and several other areas of signal processing require large order FIR filters. Since the number of multiply-accumulate (MAC) operations required per filter output increases linearly with the filter order, real-time implementation of these filters of large orders is a challenging task. Several attempts have, therefore, been made and continued to develop low-complexity dedicated VLSI systems for these filters.the below figure 2 shows the conventional memory multiplier[5].

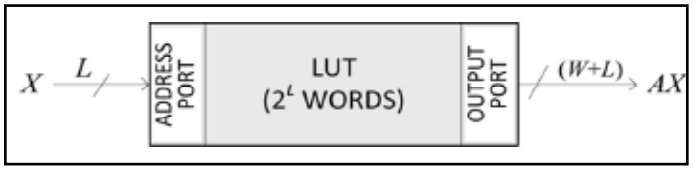

Fig. 3 : Conventional memory multiplier

C. Truncated Multiplier

Multiplication is one of the most area consuming arithmetic operations in high-performance circuits. As a consequence many research works deal with low power design of high speed multipliers. Multiplication involves two basic operations, the generation of the partial products and their sum, performed using two kinds of multiplication algorithms, serial and parallel. Serial multiplication algorithms use sequential circuits with feedbacks: inner products are sequentially produced and computed. Parallel multiplication algorithms often use combinational circuits and do not contain feedback structures[6].

Multiplication of two bits produces an output which is twice that of the original bit. It is usually needed to truncate the partial product bits to the required precision to reduce area cost. Fixed-width multipliers, a subset of truncated multipliers, compute only n most significant bits (MSBs) of the 2n-bit product for n × n multiplication and use extra correction/compensation circuits to reduce truncation errors. In previous related papers, to reduce the truncation error by adding error compensation circuits. So that the output will be précised. In this approach jointly considers the tree reduction, truncation, and rounding of the PP bits during the design of fast parallel truncated multipliers so that the final truncated product satisfies the precision requirement. In our approach truncation error is not more than 1ulp (unit of least position), so there is no need of error compensation circuits, and the final output will be précised[7].

III. Proposed FIR Filter

A. Vedic Multiplier

Multiplication is an important fundamental function in arithmetic operations. Multiplication-based operations such as Multiply and Accumulate(MAC) and inner product are among some of the frequently used Computation- Intensive Arithmetic Functions(CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT), filtering and in microprocessors in its arithmetic and logic unit. Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip.

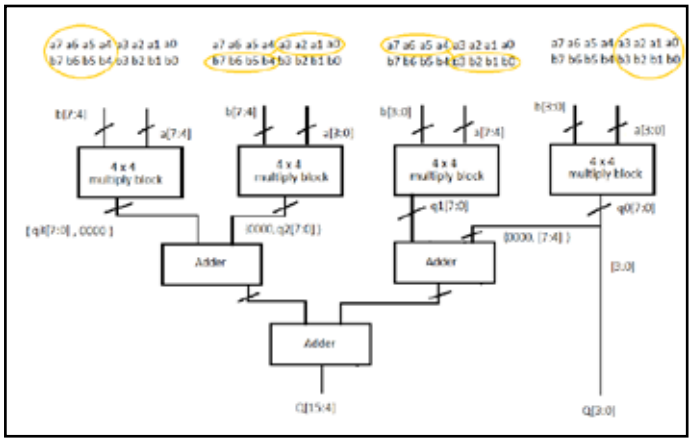

Fig. 4 : Vedic multiplier

Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and crosswise". To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (5498 × 2314). The conventional methods already know to us will require 16 multiplications and 15 additions[8].

An alternative method of multiplication using Urdhva Tiryakbhyam Sutra is shown in figure 3. The numbers to be multiplied are written on two consecutive sides of the square as shown in the figure 3. The square is divided into rows and columns where each row/ column corresponds to one of the digit of either a multiplier or a multiplicand. Thus, each digit of the multiplier has a small box common to a digit of the multiplicand. These small boxes are partitioned into two halves by the crosswise lines. Each digit of the multiplier is then independently multiplied with every digit of the multiplicand and the two-digit product is written in the common box.

All the digits lying on a crosswise dotted line are added to the previous carry. The least significant digit of the obtained number acts as the result digit and the rest as the carry for the next step. Carry for the first step (i.e., the dotted line on the extreme right side) is taken to be zero. Here, "Urdhva Tiryakbhyam Sutra" or "Vertically and Crosswise Algorithm" for multiplication has been effectively used to develop digital multiplier architecture. This algorithm is quite different from the traditional method of multiplication, which is to add and shift the partial products[9].

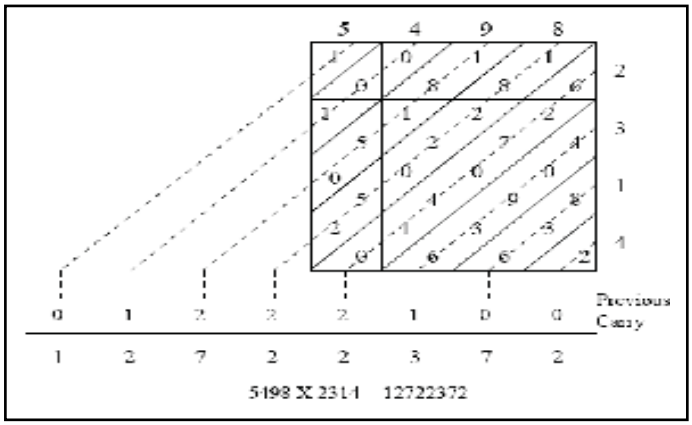

Fig. 5 : Alternative way of multiplication by Urdhva Tiryakbhyam Sutra

IV. Simulation Results

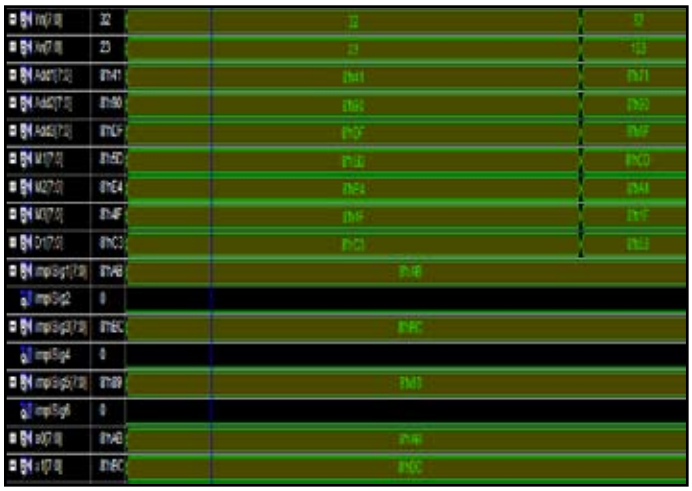

Fig. 6 : Tranposed fir filter design using truncated multiplication

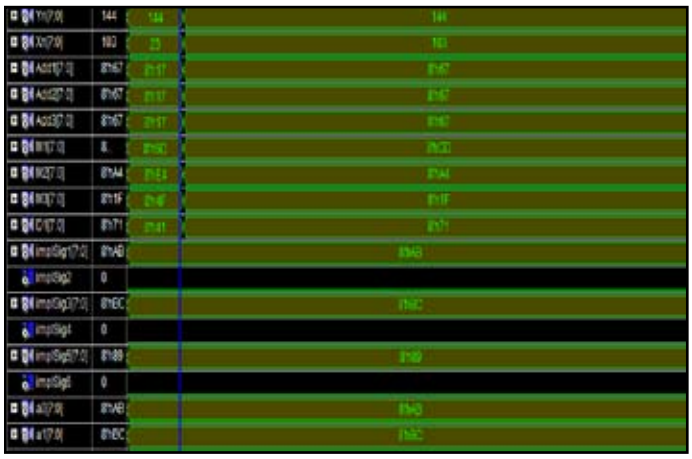

Fig.7 : Direct fir filter design using truncated multiplication

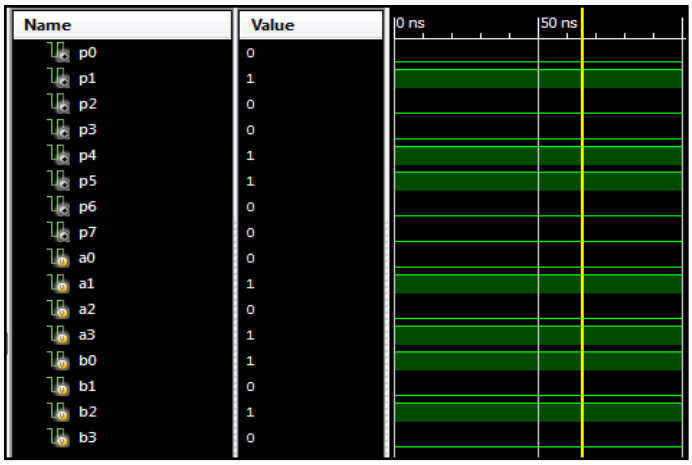

Fig. 8 : Vedic multiplication

V. Conclusion

This paper has presented low-cost FIR filter designs by jointly considering the optimization of coefficient bit width and hardware resources in implementations. By using a new truncated multiplier design by jointly considering the reduction, deletion, truncation, and rounding of the PP bits. The faithfully truncated multiplier has a total error of no more than one unit of the last place (ulp) and can be used in applications that require accurate results.

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considering the optimization of coefficient bit width and hardware resources in implementations. Although most prior designs are based on the transposed form, we observe that the direct FIR structure with faithfully rounded MCMAT leads to the smallest area cost and power consumption.

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