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Design and VLSI Simulation of SRAM Memory Cells for Multi-ported SRAM's

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Abstract

With the increasing use of portable consumer electronics, power consumption has become an important performance characteristic for a chip due to both limited battery life in portable systems and also due to expensive packages and heat sinks required by high power levels. In several applications, the embedded SRAMs can occupy the majority of the chip area and contain millions of transistors. Since RAMs are critical to processor performance, researchers have sought to optimize their performance and efficiency through reconfiguration. Firstly, the design of an SRAM cell is key to ensure stable and robust SRAM operation. Secondly, owing to continuous drive to enhance the on-chip storage capacity, the SRAM designers are motivated to increase the packaging density. This project presents the architecture and circuit design for a multi-ported SRAM building block. The SRAM cell with load (6T) and without load (4T) is going to be designed and implement in 130nm technology and comparison between them in terms of power consumed, area and access time. Electric Tool is used to design the schematic and layout level diagrams of our project. The LT-SPICE Tool will be used for simulation of the Spice code which tests the functionality of our generated layout and schematic blocks.

Keywords

SRAM, reconfiguration, SRAM register file, LT-SPICE.

I. Introduction

Memories often account for the majority of transistors in a CMOS system –on- chip. Random access memory is accessed with an address and has latency independent of the address. In contrast, serial access memories are accessed sequentially so no address is necessary to be specified. If a serial access memory is accessed at a random location then its access time varies based on the specific location[1].

Considerable attention has been given to the design of low-power and high performance SRAMs since they are critical components in both high-performance processors and hand-held portable devices. The design of high performance computer systems require SRAMs with cycle times below 5ns for the cache and control memories. With the process technology pushing well into the ultra deep sub-micron (UDSM) arena, IC designers can now integrate significant densities of memory and logic together in the same chip. Such an embedded SRAM market is even larger than stand-alone SRAM market and this memory on chip reduces cost with improved speed performance. Design of higher speed and higher density SRAMs is necessary because of their growing embedded applications.

Starting from the design specification to the generation of mask layout, layout design of an integrated circuit has several processing steps which have to be carefully exercised. These steps include design of transistor level schematic, simulation of the circuit according to the designed W/L ratios of the individual transistors, drawing of the layout using a layout editor (Electric Tool), parasitic extraction and final simulation and verification. These all processing methods are inevitable for the error free operation of chip and similar methodology is followed for the design of SRAM. Basic building block of the SRAM is SRAM cell which stores one bit data. Using common bit lines, data can be read and written to the SRAM cell[2].

Precharge circuit, sense amplifier and read-write circuits complete one SRAM memory. The memory is arranged in row-column matrix which facilitates easy addressing of memory bits and also provides design flexibility. Once the functionality of one memory cell array is proved it can be duplicated several times with minor design changes in the I/O control circuitry.

The size of a SRAM with m address lines and n data lines 2^m words or $2^m \times n$. Here each word size is n, but we designed as single bit sized word. It is too difficult to construct large bit memory directly, by keeping all cells and their decoder, other circuitry with their connections. It becomes complex and lengthy, in accurate and also time consuming. So in order to eliminate above discomforts, we constructed small modules and these modules are used in next higher module, these module is used in further module. Firstly precharge, sense amplifier, 6T SRAM cell, data enable, 2 to 4 decoder, are designed[3].

II. Sram Cell Design And Operation

Complementary metal oxide semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication. CMOS is also sometimes reffered to as complementary symmetry metal-oxide semiconductor (or COS-MOS).The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFET's) for logic functions[4].

Two important characteristics of CMOS devices are high noise immunity and low static power consumption. Since one transistor of the pair is always off, the series combination draws significant power only momentarily during switching between on and off states. Consequently, CMOS devices do not produce as much waste heat as other forms of logic. The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material.

A. Operation of CMOS 6T SRAM Cell

The SRAM cell consists of a bi-stable flip-flop connected to the internal circuitry by two access transistors. When the cell is not addressed, the two access transistors are closed and the data is kept to a stable state, latched within the flip-flop. The flip-flop needs the power supply to keep the information. The data in an

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SRAM cell is volatile (i.e., the data is lost when the power is removed)[5].

However, the data does not "leak away" like in a DRAM, so the SRAM does not require a refresh cycle. Static RAM is fast because the six-transistor configuration of its flip-flop circuits keeps current flowing in one direction or the other (0 or 1). The 0 or 1 state can be written and read instantly without waiting for a capacitor to fill up or drain (like in DRAM). However, the six transistors take more space than DRAM cells made of one transistor and one capacitor. When opposite voltages are applied to the column wires, the flip-flop is oriented in one of two directions for a 0 or 1. At that point, the flip-flop becomes a self-perpetuating storage cell as long as a constant voltage is applied.

Random access means that locations in the memory can be written to or read from read and write operations sequentially. Newer synchronous static RAM chips overlap reads and writes contrast with dynamic RAM. Generally the operation of SRAM consisting of three modes. They are:

1. Idle (standby) mode
2. Write mode
3. Read mode

The schematic of basic 6T CMOS SRAM cell is shown in the below figure 1. This cell consists of a bi-stable flip-flop connected to the internal circuitry by two access transistors.

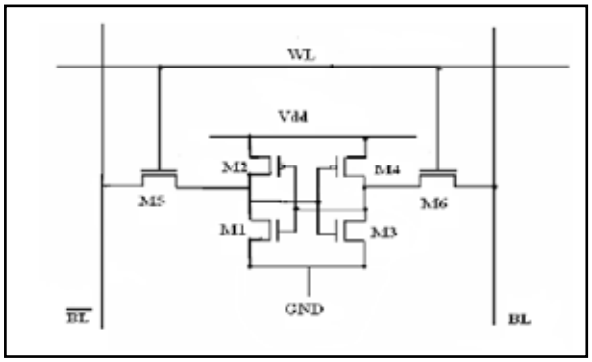

Fig. 1 : Basic 6T CMOS SRAM cell

B. Operation of CMOS 4T SRAM Cell

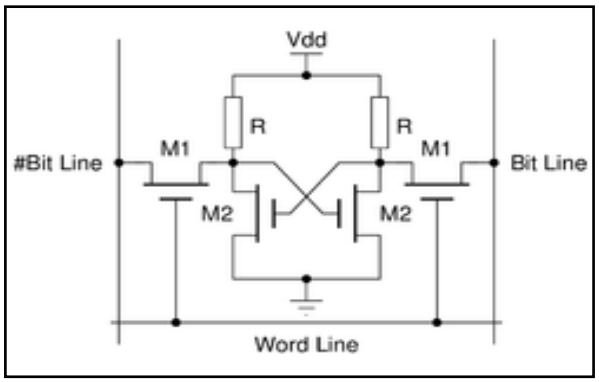

Fig. 2 : Basic 4T CMOS SRAM cell

The figure 2 shown is called 4T cell since there are now only four transistors in the cell. To minimize power, the current through the resistors can be made extremely small by using very large pull-up resistances. Sheet resistance of these resistors is 10MΩ per square or higher and the area is minimal.

Standby currents are kept in the nanoampere range. Thus, power and area may be reduced at the expense of extra processing complexity to form the undoped polysilicon resistors. However, the majority of the designs today use the conventional 6T configuration. The row select lines, or word lines, run horizontally. All cells connected to a given word line are accessed for reading or writing. The cells are connected vertically to the bit lines using the pair of access devices to provide a switchable path for data into and out of the cell. In principal, it should be possible to achieve all memory functions using only one column line and one access device[6].

Attempts have been made in this direction, but due to normal variations in device parameters and operating conditions, it is difficult to obtain reliable operation at full speed using a single access line. Therefore, the symmetrical data paths are almost always used. Row selection in CMOS memory is accomplished using the decoders. For synchronous memories, a clock signal is used in conjunction with the decoder to activate a row only when read-write operations are being performed. At other times, all word lines are kept low. When one word line goes high, all the cells in that row are selected. The access transistors are all turned on and a read or write operation is performed. Cells in other rows are effectively disconnected from their respective word lines.

Once the cells along the word line are enabled, read or write operations are carried out. For a read operation, only one side of the cell draws current. As a result, a small differential voltage develops between *b* and b-bar on all column lines. The column addresses decoder and multiplexer select the column lines to be accessed. The bit-lines will experience a voltage difference as the selected cells discharge one of the two bit-lines. This difference is amplified and sent to output buffers. It should be noted that the bit-lines also have a very large capacitance due to the large number of cells connected to them[7].

III. Multi-ported sram's

Multi-ported RAMs are essential for high-performance parallel computation systems. VLIW and vector processors, CGRAs, DSPs, CMPs and other processing systems often rely upon multi-ported memories for parallel access, hence higher performance. Although memories with a large number of read and write ports are important, their high implementation cost means they are used sparingly in designs. As a result, FPGA vendors only provide dual-ported block RAMs to handle the majority of usage patterns.

Multi-ported memories are the cornerstone of all high-performance CPU designs. They are often used in the register files, but also in other shared-memory structures such as caches and coherence tags. Hence, high-bandwidth memories with multiple parallel reading and writing ports are required[8].

In particular, multi-ported RAMs are often used by wide superscalar processors, VLIW processors, multi-core processors, vector processors, coarse-grain reconfigurable arrays (CGRAs), and digital signal processors (DSPs). For example, the second generation of the Itanium processor architecture employs a 20-port register file constructed from SRAM bit cells with 12 read ports and 8 write ports. The key requirement for all of these designs is fast, single-cycle access from multiple requesters. These multiple requesters require concurrent access for performance reasons.

A multi-port is a static RAM with a dual-port or multi-port cell. Each port has separate address, data and control signals for accessing a common SRAM array. Infact there are single port memory cells are available, instead we are moving our interest from these to higher end i.e multi-ported RAMs (MRAMs).

The differences between standard Static Random Access Memory (SRAM) and Multi-Port SRAM are very straightforward. A

standard SRAM has only one port which consists of an address bus, data bus and control bus. The address bus allows any location in the memory array to be uniquely identified. The control bus tells the array whether the data on the data bus is to be written into the location or the data in the location is to be read out on the data bus. The Multi-Port SRAM will have two or more ports. Again each port will have an address bus, data bus and control bus. Each port has the capability to address any location in the memory array and write data in or read data out. Some of these devices are available in asynchronous (all timing controlled by the CPU) or synchronous (timing provided by a master clock) formats.

IV. Schematic and Simulation Results

The below figures 3 and 4 shows the schematic and simulation results for the basic Single-port CMOS 6T SRAM cell(4*4).

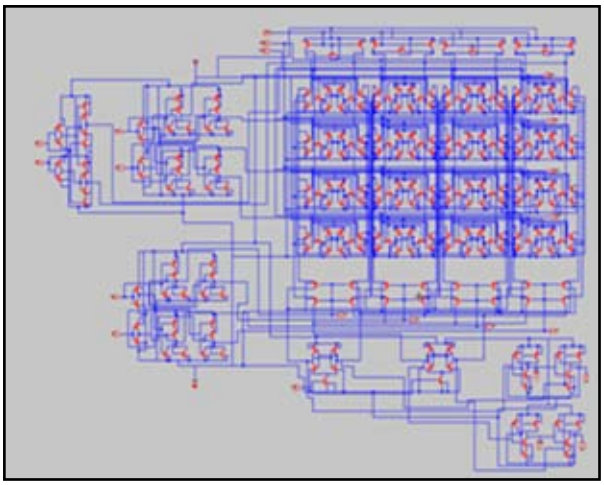

Fig. 3 : Schematic for Multi-port CMOS 6T SRAM cell (4*4)

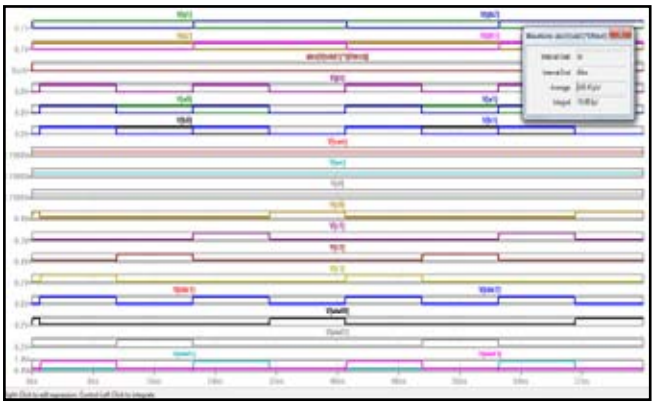

Fig. 4 : Simulation result for Multi-port CMOS 6T SRAM cell (4*4)

The below figures 5 and 6 shows the schematic and simulation results for the basic Single-port CMOS 4T SRAM cell (4*4).

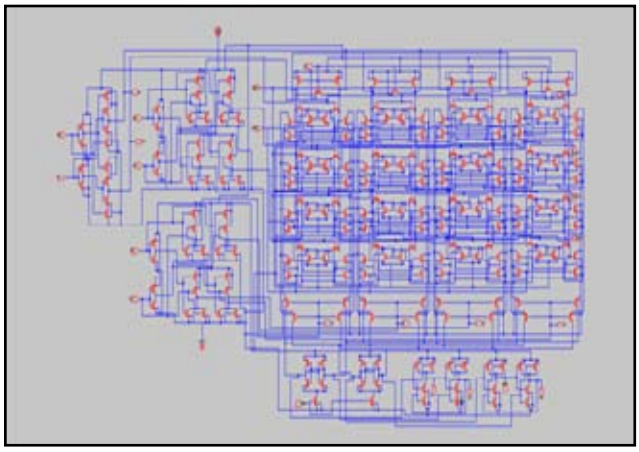

Fig. 5 : Schematic for Multi-port CMOS 4T SRAM cell(4*4)

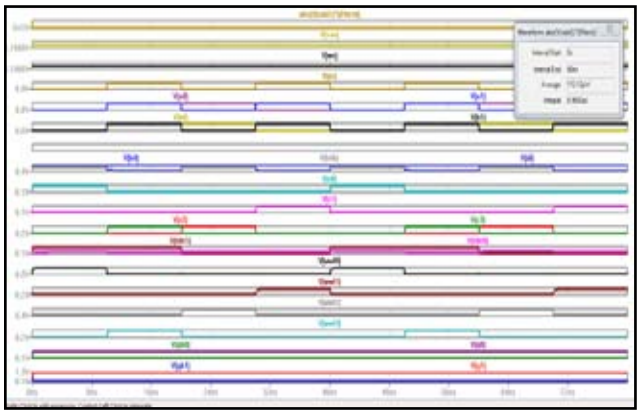

Fig. 6 : Simulation result for Multi-port CMOS 4T SRAM cell(4*4)

V. Table

The below table shows the Comparison in terms of Power Consumption, Access time and Area.

Power(in watts)	Area(no. of transistors)	Access Time(ns)	Write	Read
Single-port 6T SRAM(1-bit)	61.45µw	31	0.26	0.20
Single-port 4T SRAM(1-bit)	48.66µw	29	0.03	0.15
Single-port 6T SRAM(4-bit)	90.91µw	68	0.10	1.97
Single-port 4T SRAM(4-bit)	53.05µw	60	0.06	0.15
Multi-port 6T SRAM(16-bit)	249.4µw	266	0.05	0.17
Multi-port 4T SRAM(16-bit)	112.1µw	234	0.03	0.13

VI. Conclusion

The 16X4 SRAM register file with 2 read ports and one write port is designed and simulated with 130 nm. The design is implemented at both schematic and layout level. The simulation results are verified for all the basic blocks and also the top level (complete SRAM register file) schematic is simulated and results are verified for all the read and write operations (two read ports and write port).

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