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Implementation of QAM Transceiver Architecture for Carrier Recovery by Using DPLL on FPGA

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Abstract
Wimax is an emerging and promising technology to provide high speed broadband connectivity to the mobile phone using latest modulation and multiplexing techniques. Wimax mainly uses QAM modulation technique due to its spectrum efficiency and several other added advantages. In such Wimax communication systems, synchronization which consists of both carrier and symbol level is the most challenging task. There have been several researchers paying attention to solve synchronization problem in particular, hence build a whole communication system.
The FPGA technology has been playing a considerable role in portable and mobile communication. This is due to the features of flexibility, accuracy and configurability in designing and implementation. This paper presents a complete design for a 16-QAM transmitter and receiver based on VHDL. The implemented system can be used in typical Wimax system and any other QAM based communication systems. The carrier synchronization and timing synchronization both issues are covered in the implementation.
The transmitter of QAM consists of symbol mapper, NCO and modulator blocks. The NCO is used for carrier generation. The receiver of QAM consists of NCO, carrier synchronization block, time synchronization block, symbol demapper and clock managing unit. All blocks will be realized in VHDL and will be aimed to implement with generic feature so that the designs are scalable for different bit sizes.

Keywords
Xilinx, Modelsim, 16-QAM, DDS, WIMAX

I. Introduction

Quadrature Amplitude Modulation or QAM is a type of modulation which is broadly utilized for modulating information signals onto a carrier utilized for radio communications. It is generally used because it offers advantages over different types of data modulation, for example, PSK, although many types of information modulation operate along side each other.
Quadrature Amplitude Modulation, QAM is a signal in which two carriers shifted in phase by 90 degrees are modulated and the resultant output comprises of both amplitude and phase variations. In perspective of the way that both amplitude and phase variations are available it might also be considered as a mixture of amplitude and phase modulation.
Quadrate amplitude modulation (QAM) may exist in what may be termed either analogue or digital formats. The analogue types of QAM are typically used to permit various analogue signals to be carried on a single carrier. For example it is used in PAL and NTSC television systems, where the distinctive channels provided by QAM enable it to carry the components of chroma or colour data. In radio applications a system known as C-QUAM is utilized for AM stereo radio. Here the distinctive channels enable the two channels needed for stereo to be carried on the single carrier.
Digital formats of QAM are often referred to as "Quantized QAM" and they are being increasingly used for data communications often within radio communications systems. QAM, Quadrature amplitude modulation is widely used in many digital data radio communications and data communications applications.

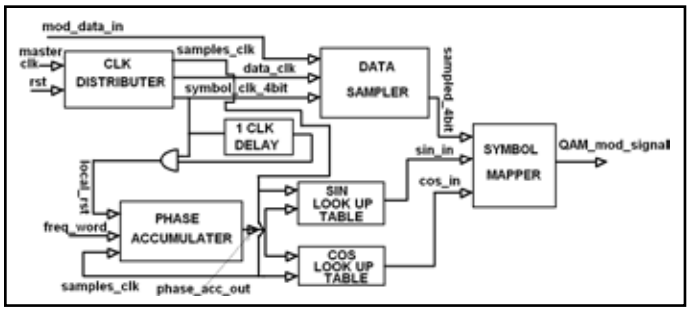

Fig. 1 : Block diagram of QAM Modulator

Block diagram of QAM modulator is given above every block is explained below in detail.

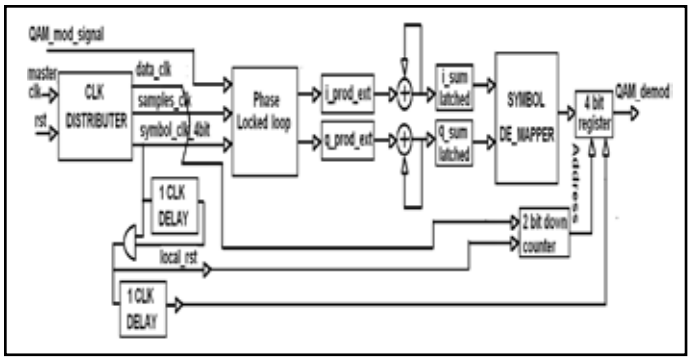

Fig. 2 : Block diagram of QAM Demodulator

II. Implementation

A. QAM transceiver using DPLL

The inputs for the clock generation module is reset and master clock of 50Mhz and the outputs are sample clock, data clock and symbol clock. The sample clock is same as the master clock. The clock generation module consists of 9 bit counter. In the counter 7th bit value gives the output of data clock and the 9th gives the output of symbol clock. The data clock will be at active low for

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128 clock pluses and for other 128 clock pluses will be in active high to complete one cycle. Symbol clock will be at active low for 512 clock pluses and for other 512 clock pluses will be in active high to complete one cycle.

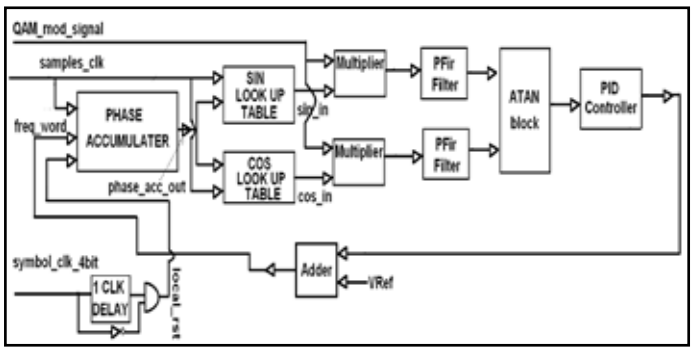

Fig. 3 : Phase locked loop block diagram

Phase locked loop is used to correct the signal at demodulator it's plays a key role in demodulation. Reset is used to clear or reset module, data clock will be four times faster then symbol clock 4bit when reset is active high then left shift register will be cleared, if reset is active low with raising edge of data clock then data input will be forced on to the LSB bit of left shift register. Left shift register will be shifter one bit. Raising edge of symbol clock 4bit then left shift register will be reflected on the output sampled 4bit.

Sampled_4bit data is loaded into a tempary register there 0^{th} bit and 1^{st} bit are assumed as I bits and 2^{nd} and 3^{rd} bit are asumed as Q bits, these I bits and Qbits are assumed as address to 3 bit Rom block's in this according to Rom address data in that address will be given to the next block called as multipler's. I bits are multipled with cos_in bits and Q bits are multipled with sin_in bits than resultant output's of the multipler section will be added which generates the final output as QAM_mod_signal.

B. Carrier recovery with DPLL

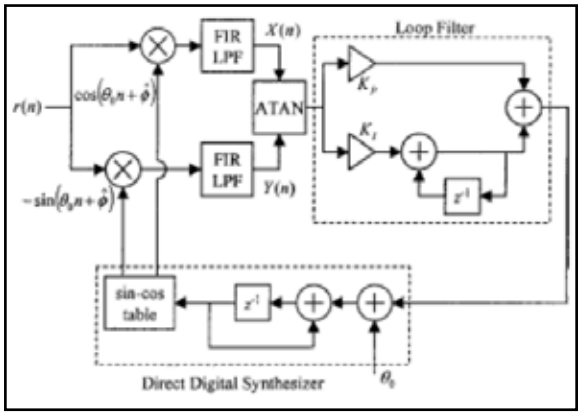

Fig. 4 : Block diagram of Carrier recovery with DPLL

The input's are I_sum and Q_sum these are trunketed to 10 bits, the MSB of trunckted is used as a select if bit is '1' then output will be same if bit is '0' then output will be negative ot the input. The generated signal is compared with threshold resultant is less then threshold then active high signal is stored in 1^{st} bit of register and 0^{th} bit will be the sel signal value. Same process will be done for I_bits and resultant will be stored in 3^{rd} and 4^{th} bits. the register of 4 bit's will be reflected as symbol_4bit.

III. Simulation Results

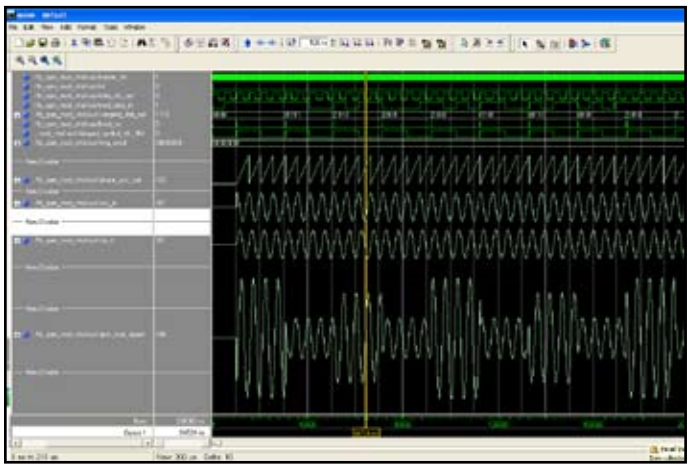

Fig. 5 : QAM modulation simulation results

Master_clock is 50MHz clock that is board clock, rst is used to reset QAM modulation module. Data_clock_out is used to collect data from mod_data_in after completing of 4 clock pluses of Data_clock_out resultant will be forced on sampled_4bit_out, delayed_sym_clock_out_4bit is used to generate local_rst this is used to reset phase_acc_out is added with freq_word and updated in phase_acc_out that will be given to cos and sin lut that generates cos_in and sin_in. processing(i.e. multiplication and addition) of combination of cos_in, sin_in and sampled_4bit_out will generate QAM_mod_signal.

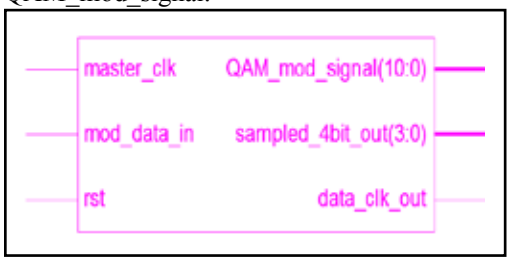

Fig. 6 : QAM Modulator Logic Symbol

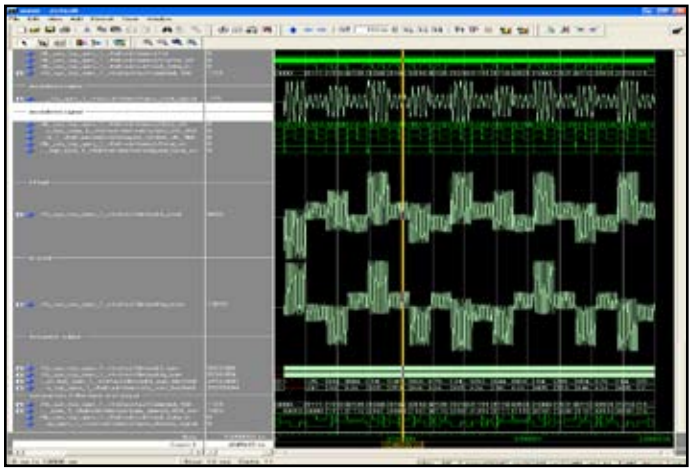

Fig. 7 : QAM demodulation simulation results

Here we are showing the QAM modulation and demodulation signals by implementing in vhdl.

IV. Chip Scope Results

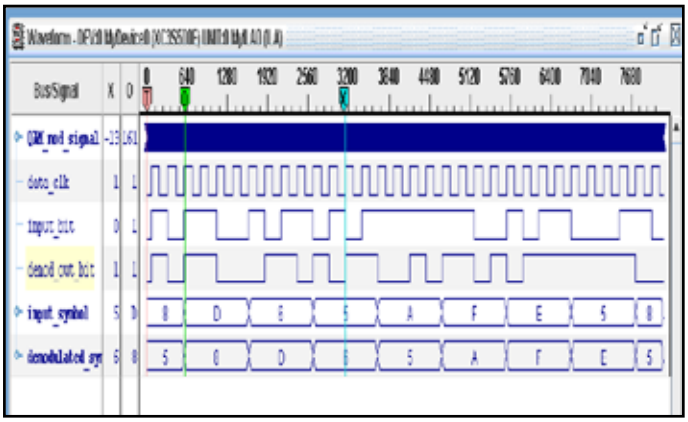

Fig. 8 Chipscope results

V. Table

Logic utilization	used	available	utilization
Number of slice flipflops	51	9,312	19%
Number of 4 input LUT's	210	9,312	9%
Number of occupied slices	134	4,656	24%
Number of bonded IOB's	19	232	9%
Number of GCLOCK'S	1	24	4%

VI. Conclusion

In this paper we implemented 16-QAM modulator and demodulator on SPARTAN 3E FPGA XC3S500E. The present design is prototyped to Spartan series FPGA. We can scale up the modules for better performance and implement on Virtex series FPGA. The present technique is designed for co-operative communication type. In future the techniques can be implemented for non-cooperative communication scheme (military applications). This can be extended for implementing 64 QAM, to support later versions of WiMAX.

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