ISSN : 2348 - 9065 (Online)
ISSN : 2349 - 3143 (Print)
Vol. 2, Issue 3 July - Sept. 2015
International Journal of Research in Electronics and Communication Technology (IJRECT 2015)

FPGA Implementation of OFDM Modulator and Demodulator for Communication Applications

[I]K.Rani, [II]J. Lingaiah, [III]G.Kalyan

Abstract

The new mobile technologies trying to give broadband over wireless channel allowing the user to have bandwidth connectivity even inside moving vehicle. The metropolitan broadband wireless networks require a non-line-of-sight (NLOS) capability, and the scheme Orthogonal Frequency Division Multiplex (OFDM) becomes essential to overcome the effects of multipath fading.

Orthogonal Frequency Division Multiplexing (OFDM) has become very popular, allowing high speed wireless communications. OFDM could be considered either a modulation or multiplexing technique and its hierarchy corresponds to the physical and medium access layer. A basic OFDM modulator system consists of a PSK modulator, a serial to parallel, and an IFFT module. The iterative nature of the IFFT and its computational order makes OFDM ideal for a dedicated architecture outside or parallel to the main processor. The VHDL implementation allows the design to be extended for either FPGA or ASIC implementation, which suits more for the Software Defined Radio (SDR) design methodology.

In this project the OFDM modulator and demodulator will be implemented with full digital techniques. VHDL will be used for RTL description and FPGA synthesis tools will be used for performance analysis of the proposed core. The major blocks are Interleaving/ Mapping circuit, 8 point IFFT, 8 point FFT, and arithmetic blocks.

Keywords

NLOS, OFDM, PSK, FFT. IFFT, VHDL, FPGA, RTL.

I. Introduction

Recently, a worldwide convergence has occurred for the use of Orthogonal Frequency Division Multiplexing (OFDM) as an emerging technology for high data rates. In particular, many wireless standards (Wi-Max,IEEE802.11a, LTE, DVB) have adopted the OFDM technology as a mean to increase dramatically future wireless communications. OFDM is a particular form of Multi-carrier transmission and is suited for frequency selective channels and high data rates. This technique transforms a frequency-selective wide-band channel into a group of non-selective narrowband channels, which makes it robust against large delay spreads by preserving orthogonality in the frequency domain.

The telecommunications industry faces the problem of providing telephone services to rural areas, where the customer base is small, but the cost of installing a wired phone network is very high. One method of reducing the high infrastructure cost of a wired system is to use a fixed wireless radio network. The problem with this is that for rural and urban areas, large cell sizes are required to obtain sufficient coverage. These results in problems cased by large signal path loss and long delay times in multipath signal propagation.

The principles of OFDM have been in existence for several decades. However, in recent years these techniques came into practice in modern communications system. Orthogonal frequency division multiplexing (OFDM) is such a technique which provides an efficient means to handle high speed data streams on a multipath fading environment that causes ISI. The required bit rates are achieved due to OFDM multicarrier transmissions. OFDM systems perform better than single carrier systems particularly in frequency selective channels. FFT (Fast Fourier Transform)/ (Inverse Fast Fourier Transform) IFFT are the main blocks in OFDM system. They are important in achieving high speed signal processing. FFT helps to transform the signal from time domain to frequency domain where filtering and correlation can be performed with fewer operations. Nevertheless, for real time systems the execution speed is the main concern. The OFDM hardware implementation has been done either on ASICs, Virtex based FPGA. ASIC based designs suffer from more time to market factor, high cost and provide less flexibility. Moreover, DSP based designs can only support limited data rates due to lack of parallelism and also they have less number of MAC(multiply and accumulate) units. On the other hand, the modern programmable circuits like an FPGA provides parallel processing system, putting the FPGA computing speed at a significant advantage over DSPs.

Figure 1 shows the configuration for a basic OFDM transmitter and receiver. The signal generated is at base-band and so to generate an RF signal the signal must be filtered and mixed to the desired transmission frequency.

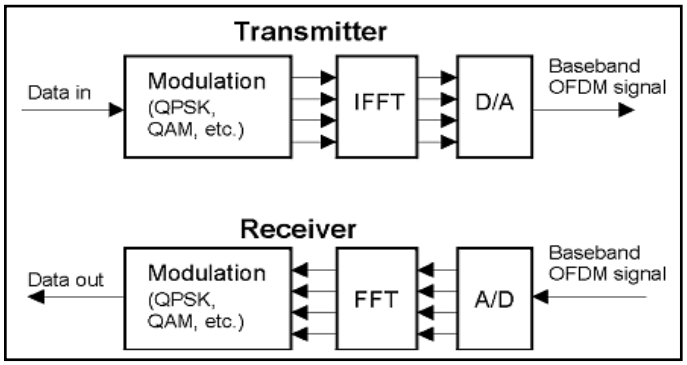


Fig.1 : Basic FFT, OFDM transmitter and receiver

With the rapid growth of digital communication in recent years, the need for high-speed data transmission has been increased. The mobile telecommunications industry faces the problem of providing the technology that be able to support a variety of services ranging from voice communication with a bit rate of a few kbps to wireless multimedia in which bit rate up to 2 Mbps. Many systems have been proposed and OFDM system has gained much attention for different reasons. Although OFDM was first developed in the 1960s, only in recent years, it has been recognized as an outstanding method for high-speed cellular data communication where its implementation relies on very high-

ISSN : 2348 - 9065 (Online)
ISSN : 2349 - 3143 (Print)

speed digital signal processing. This method has only recently become available with reasonable prices versus performance of hardware implementation.

Since OFDM is carried out in the digital domain, there are several methods to implement the system. One of the methods to implement the system is using Field-Programmable Gate Array (FPGA).This hardware is programmable and the designer has full control over the actual design implementation without the need (and delay) for any physical IC fabrication facility. An FPGA combines the speed, power, and density attributes of an ASIC with the programmability of a general purpose processor will give advantages to the OFDM system. An FPGA could be reprogrammed for new functions by a base station to meet future needs particularly when new design is going tofabricate into chip. This will be the best choice for OFDM implementation since it gives flexibility to the program design besides the low cost hardware component compared to others.

II. Implementation

To generate OFDM successfully the relationship between all the carriers must be carefully controlled to maintain the orthogonality of the carriers. For this reason, OFDM is generated by firstly choosing the spectrum required, based on the input data, and modulation scheme used. Each carrier to be produced is assigned some data to transmit. The required amplitude and phase of the carrier is then calculated based on the modulation scheme (typically differential BPSK, QPSK, or QAM). The required spectrum is then converted back to its time domain signal using an Inverse Fourier Transform. In most applications, an Inverse Fast Fourier Transform (IFFT) is used. The IFFT performs the transformation very efficiently, and provides a simple way of ensuring the carrier signals produced are orthogonal. The Fast Fourier Transform (FFT) transforms a cyclic time domain signal into its equivalent frequency spectrum. This is done by finding the equivalent waveform, generated by a sum of orthogonal sinusoidal components. The amplitude and phase of the sinusoidal components represent the frequency spectrum of the time domain signal. The IFFT performs the reverse process, transforming a spectrum (amplitude and phase of each component) into a time domain signal. An IFFT converts a number of complex data points, of length that is a power of 2, into the time domain signal of the same number of points. Each data point in frequency spectrum used for an FFT or IFFT is called a bin.

The orthogonal carriers required for the OFDM signal can be easily generated by setting the amplitude and phase of each frequency bin, then performing the IFFT. Since each bin of an IFFT corresponds to the amplitude and phase of a set of orthogonal sinusoids, the reverse process guarantees that the carriers generated are orthogonal.

A. Design of OFDM transmitter

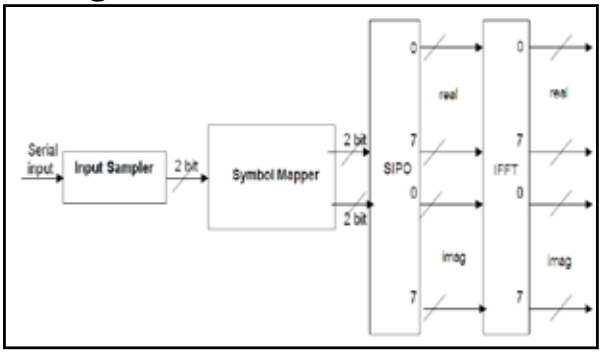


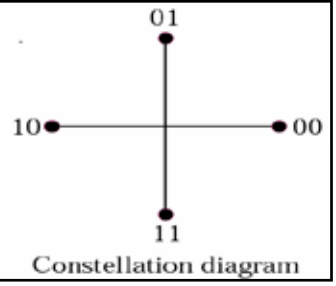
Fig. 2 : OFDM transmitter

Input Sampler IQ Gen: This block samples the serial input and generates 2 bit IQ output.

Symbol Mapper: This block maps the input I, Q to the corresponding to the real part and imaginary part of the constellation symbols.

Dibit	Phase
00	0
01	90
10	180
11	270

Dibit (2 bits)



Constellation diagram

Fig.3 : Constellation diagram

SIPO: This block converts the serial input to the parallel output. This block is used in OFDM TX, to convert serial input to parallel output. This block's output is given to the input of IFFT.

B. Design of OFDM receiver

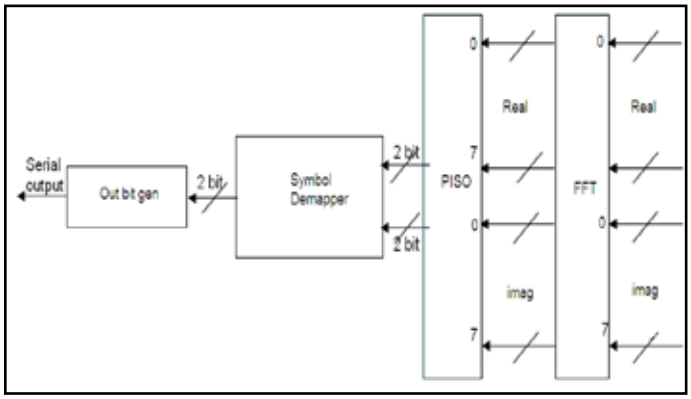


Fig.4 : OFDM receiver

PISO: This block converts the parallel input to the serial output. This block is used in OFDM RX, to convert parallel input to serial output. This block's output is given to the Symbol demapper.

Symbol demapper: This block maps, the Real and imaginary parts of the serial out from PISO, to the IQ corresponding to the real part and imaginary part of the constellation symbols. It extracts the IQ values from the serial out of PISO.

Out bit generator: This block takes 2 bit IQ s from Symbol demapper and generates output bits.

Clock distributor: This is the clock distributor block, which generates two enable signals en_div_2 and en_div_16.en_div_2 is divided by 2 of input clock.en_div_16 divided by 16 of input clock.

III. Simulation Results

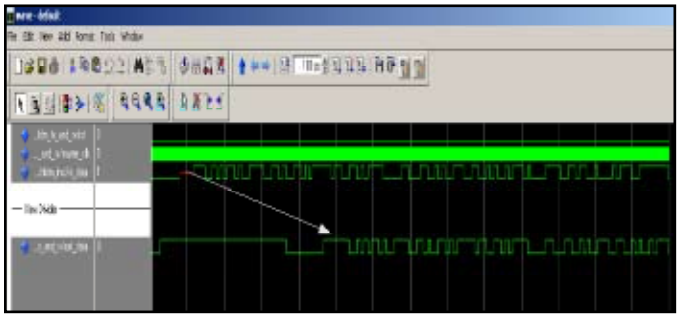


Fig.5 : OFDM final output

IV. Chipscope Results

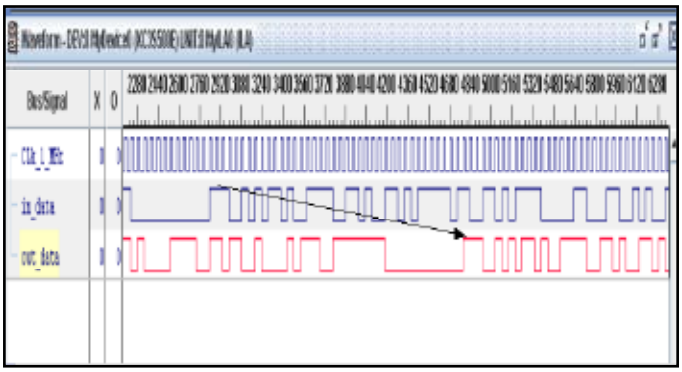


Fig.6 : OFDM chipscope results

V. Conclusion

In this paper, OFDM MODEM has been studied and implemented for Modulator and Demodulator and Its applications have been extended from high frequency radio communications to telephone networks, digital audio broadcasting and terrestrial broadcasting of digital television. The advantages of OFDM, especially in the multipath propagation, interference and fading environment, make the technology a promising alternative in digital communications including mobile multimedia. Therefore this design can be applied to real-time signal processing system, which completes the main computing modules in the OFDM for multi services.

The capability of designing and implementing an OFDM MODEM is presented in this work,the design considered using a pure VHDL with the aid of IPs to implement the IFFT and clock Synthesis Function , from the Mapping results the design can be easily fit into Xilinx FPGA XC3S500E.

References

[1] *Lenin Gopal*, Daniel Wong Sing Tze, Nur Zawanah Ishak "Design of an FPGA-Based OFDM Transceiver "for DVB-T Standard, School of Engineering and Science, Curtin University Sarawak Malaysia Miri, Sarawak, Malysia .*

[2] *On the design of an "FPGA-Based OFDM modulator" for IEEE 802.16-2004, Joaquín García, René Cumplido, Department of Computer Science, INAOE, Puebla,Mexico, joaquingr@ccc.inaoep.mx.*

[3] *E.Lawrey, Multiuser OFDM, in Proc. International Symposium on Signal Processing Applications '99 vol2, 1999, pp.761.764.*

[4] *Ahmad sghaier,Shawki Areibi and Bob Dony, School of Engineering, Guelph, Guelph ON Canada N1G2W1, A Pipeline Implementation Of OFDM Transmission On Reconfigurable Platforms.*

[5] *Joaquín García, René CumplidoDepartment of Computer Science, INAOE, Puebla, Mexico On the design of an FPGA-Based OFDM modulator forIEEE 802.16-2004jo, rcumplido@inaoep.mx.*

[6] *Fundamentals of Wireless communication by David Tse and Pramod Vishwanath.*

Authors Profile

K. RANI is presently pursuing final semester M. Tech in VLSI at Arjun College of Technology and Sciences, Batasingaram village, Hayathnagar, R.R. Dist, Hyderabad, Telangana, India. E-Mail: kodaganti.rani@gmail.com

J. LINGAIAH is presently working as Head of Department in the department of Electronics and Communication Engineering in Arjun College of Technology and Sciences, Batasingaram Village, Hayathnagar, R.R. Dist, Telangana, India. E-Mail: hodeceacts@gmail.com

G. KALYAN is presently working as Application Engineer in Unistring Tech Solutions Pvt Ltd, Hyderabad, Telangana, India. E-Mail: kalyan@unistring.com