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A Study of CMOS Cell for Low Power Consumption VLSI Application

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Abstract
VLSI is a very large scale integration process of creating an integrated circuit by combining thousands of transistors into a single chip. It is very useful for complex semiconductor and communication technologies. New generation of processing technology are being developed while present generation devices are at very distance from the fundamental physical limits. A need for power VLSI chip arises from such evolution forces of integrated circuits. The intel4004 microprocessor, developed in 1971, had 2300 transistors, dissipated about 1 watts of power and clocked at 1Mhz. Therefore, a CMOS cell must be as small as possible while meeting the stability, speed, and power constraints. Third, the cell layout largely determines the CMOS area, which is the chip yield limiter. Meeting the design constraints requires deeper understanding of the involved trade-off. The main source of power dissipation in these high performance battery-portable digital systems running on batteries such as note-book computers, cellular phones and personal digital assistants are gaining prominence system, low power consumption is a prime concern, because it directly affects the performance by having effects on battery longevity. In this situation, low power VLSI based CMOS chip design has assumed great importance as an active and rapidly developing field.

Keywords
CMOS cell, Decoder, Power, Energy , Sense Amplifier, Pre-charge circuit.

I. Introduction

Energy & Power - The power consumed by a device is, by definition, the energy consumed per unit time. In other words, the energy (E) required for a given operation is the integral of the power (P) consumed over the operation time (T), hence

$$E = \int_0^T P(t)dt \qquad (1)$$

Here, the power of digital CMOS circuit is given by

$$P = C V_{DD} V_S f \qquad (2)$$

Where, *C* is the capacitance being recharged during a transition. V_{DD} is the supply voltage, V_s is the voltage swing of the signal, and f is the clock frequency. If it is assumed that an operation requires *n* clock cycles, T can be expressed as n / f. Hence, Equation (1) can be rewritten as

$$E = n C V_{DD} V \qquad (3)$$

It is important to note that the energy per operation is independent of the clock frequency. A basic CMOS cell consists of two cross coupled inverters which act as a simple latch as storage elements and two switches connecting these two inverters to complementary bit lines to communicate with the outside of the cell (figure 1)

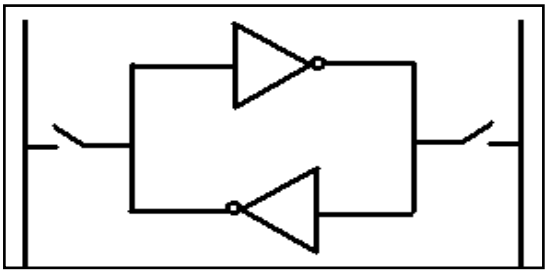

Fig. 1: Basic chip cells [5]

Two switches in figure 1 are NMOS pass-transistors, which are controlled by a word line. As long as the pass-transistors are turned off, the cell keeps one of its two possible steady states. The structure shown in figure 1 is symmetric and both bit lines BL and *BL* take part in read and write operations. Common word line (i.e., WL) controls accessibility to the cell nodes Q and QB through two-pass transistor during reading or writing. To perform the write operation into CMOS cell, the value and its complements are loaded onto the bit lines by write circuit and the word line is raised simultaneously. To read a value from a CMOS cell, both bit lines are precharged high and the word line is raised turning on the pass transistors. The bit line relative to the cell node that contains 0 begins discharging. The sense amplifier, which is connected to the bit lines, detects which of the bit lines is discharging and hence reads the stored value. The CMOS Cell is shown below in fig: 1.2.

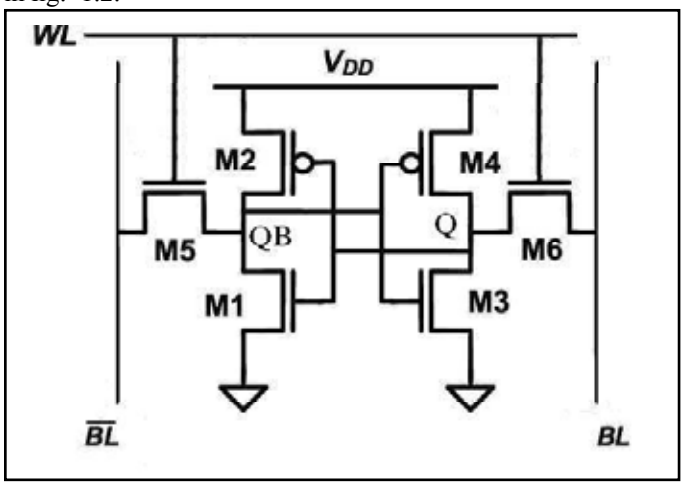

Fig.1.2 : CMOS Cell [3]

II. Operation of CMOS Cell

Assume that we want to read '1' means a 1 is stored at Q node and a 0 is stored at QB. Also, assume that both bit lines are precharged to

Vdd before the read operation to be performed. The read operation should be started by asserting the word line, which enables the two pass-transistors M 5 and M 6 (see figure 1.2). Consequently, the contents stored at Q and QB begins to transfer to the bit lines BL and *BLB* respectively. BL remains at its precharge value while *BLB* will be pulled down to the ground by discharging through M5 -M1. A careful attention should be paid in sizing of transistors to prevent unexpected writing a zero into the cell. This is illustrated in figure 1.3. Consider the *BL* side of the cell. The capacitance of the bit line for larger memories is significant. Upon enabling the WL, initially *BL* stays in its precharged value Vdd. The path composed of M5 -M1 pulls down the bit line towards ground. As we would like to have a minimum size cell, these transistors should be chosen as close to minimum as possible, which cause slow discharge of bit line capacitance. Immediately when a small difference is created.At the beginning, when the word line is rising, the intermediate, QB, is pulled up toward the precharge value of bit line, *BLB*. This voltage rise must be kept as low as possible

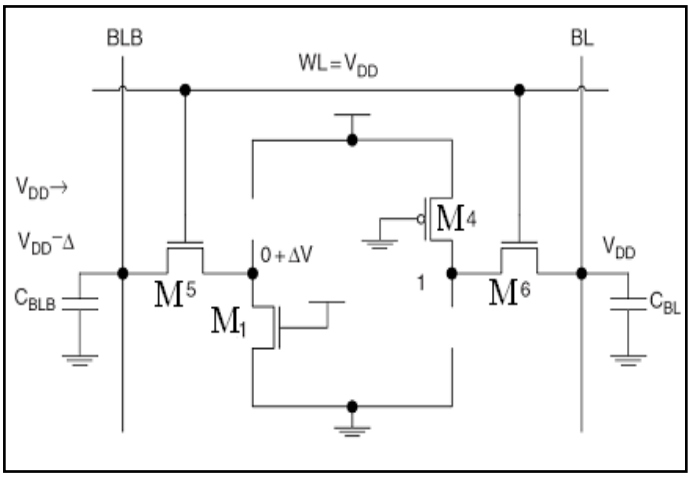

Fig. 1.3 : Read Operation of CMOS Cell [3]

with careful sizing of transistors not to cause sufficient current derive through M_3 -M_4 inverter, which may cause flip in the cell state. To avoid this from happening, the resistance of pull-down transistor, M_1, must be less than that of pass transistor M_5. This can be quantitatively obtained by solving the current equation at the maximum allowed value of voltage rise at node QB, which is the transistor threshold (of about 0.3 V). In other words, having less resistance for M_1, it must be stronger than access pass transistor. This means that the following relation must be satisfied.

$$\beta = CR = \frac{W_1/L_1}{W_5/L_5}$$

Assuming M_1 as minimum size transistor, the access pass transistor M_5 has to be made weaker by increasing its length. This is undesirable, because it adds to the capacitance of bit line. Hence, it is favorable to minimize the size of M_5 and increase the width of pull-down M1 to fulfill the stability requirements.

Sense Amplifier: The major issue in the design of CMOSs chip is the chip access time (or speed of read operation). For high performance CMOSs, it is essential to take care of the read speed both in the cell-level design and in the design of a sense amplifier. Since sense amplifiers are one of the most critical circuits in CMOS memories. So their performance strongly affects both chip access time and also overall power consumption of the chip. A high-density chip contains commonly increased bit line parasitic capacitances. These capacitances make the voltage sensing slow and bit line voltage swings energy consuming that result more power consuming memories. Need for larger chip capacity, higher speed, and lower power dissipation impose trade offs in the design of sense amplifier. Increase in number of cells per bit line increases the bit line parasitic capacitance. Decreasing cell area to integrate more chip on a single chip reduces the current that is driving the heavily loaded bit line. This causes smaller voltage swing on the bit line. Now decreasing the voltage lead to smaller noise margin that affects the sense amplifier reliability.

III. Function of Row and Column Decoders in CMOS Cell

The function of the row and column decoder is to selects a particular chip location in the array based on binary address of the row and column [5]. The row decoder selects one of the 2^n word line based by raising its voltage while column decoder selects one of the 2^m bit lines of the ROM array according to the M-bit column address, and route the content of data of the selected bit line to the output. The NOR based decoders are used both for row and column decoders. It works like dynamic circuit and requires a pre-charge cycle followed by the evaluation stage.

Pre-charge state: When the 'Pre-charge' input is applied, the PMOS devices turn ON and all the outputs of the decoder go to V_{dd} (Logic '1'). After the pre-charge is done, PMOS device turns OFF but the outputs will remain at Logic '1', because the charge is stored on the capacitors. Now when the inputs are applied on the address lines the corresponding NMOS devices will become turned ON and the charged capacitor on that line will be started to discharge to ground. Therefore only one, except all line will remain at V_{dd} (Logic '1'). The line, which remains high, will be the decoded line and this line will drive all the NMOS transistors on that line. Thus the right data will be available on the data line. This data will be given to the output data block, which will return the correct data to the outside world when the OE (Output Enable) signal is asserted.

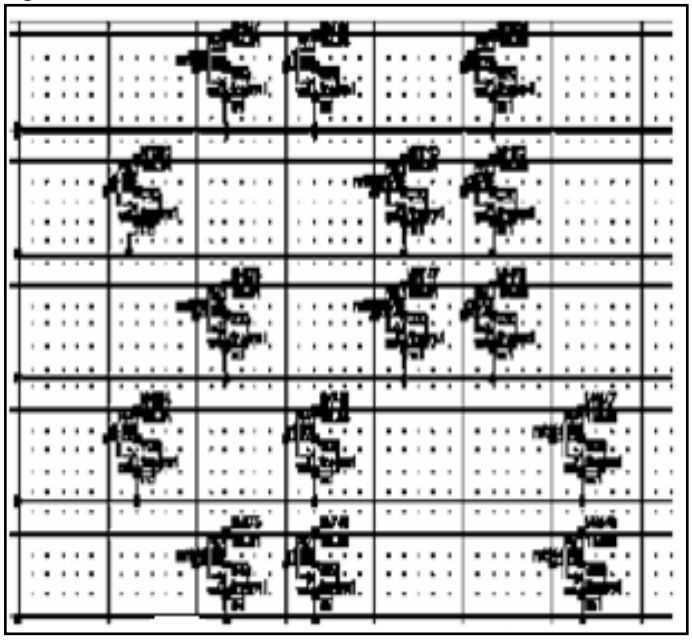

Fig. 1.4 : Dynamic NOR Decoder [2]

IV. Precharge Circuit in CMOS CELL

The main function of the Precharge circuit is to equalized voltage on both blb and bl. In both read and write operations, the bit lines

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are initially pulled up to a high voltage near V_{DD}. The precharge circuit is used to precharge the bit lines depending on the type of sensing which is used in the read operation. A precharge signal, pcb, is applied to the two pull-ups the two bit lines. When the word line (wl) signal goes high, one bit line remains high and the other falls at a linear rate until wl goes low. The difference between the bit lines is given into a voltage-sensing amplifier, which is triggered when the differential voltage exceeds a certain threshold. The schematic of the precharge circuit is shown in the fig

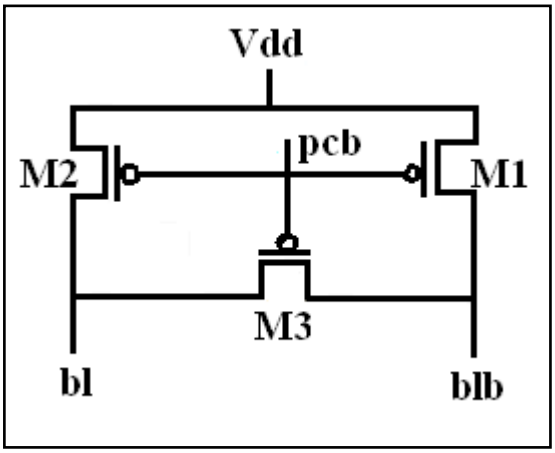

Fig. 1.5 : Precharge circuit [4]

The main reason of power consumption during high V_{dd} is time window of transition region are large so device take more time to short between Vdd and ground. It will be computed from the formula $P= CV^2F$. In the case of CMRR it value should be high for any amplifier. Same thing is also applicable for sense

Table: 1 Delay and Power Dissipation with varying Supply Voltage

S.NO.	Delay (nS)	Power(W)	Vdd (V)
1	12.376	5.2809	1
2	7.249	20.0251	2
3	3.347	47.3607	3
4	1.162	92.4523	4
5	0.852	160.8958	5

Amplifier Speed of sense amplifier increases when CMRR increases. The reason behind that better CMRR helps to suppressed common mode signal

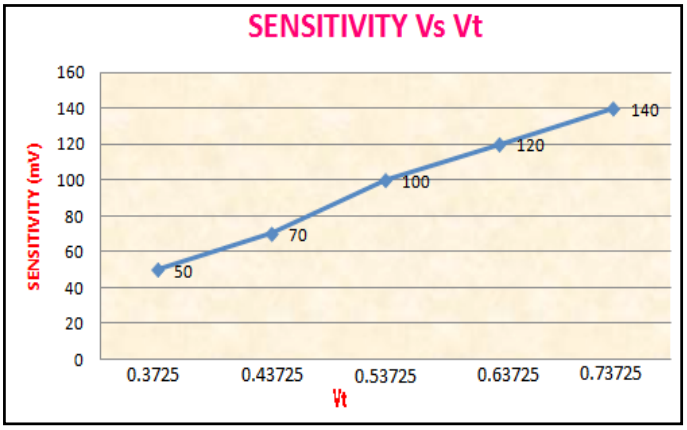

Fig. 1.5 : Vraiation of Sensitivity according to Vtn

Sensitivity is the minimum detectable signal that is detected by the sense amplifier. It is clear that when threshold voltage of the differential pair of sense amplifier increases, sensitivity also increases.

V. Conclusions

In this paper we have designed a CMOS cell, differential voltage sense amplifier, precharge circuit, 2:4 block decoder , row decoder & column decoder, chip circuits both containing chip bank and without chip bank and simulate all these circuit using VLSI technology. In sense amplifier CMRR, delay and power are calculated for different value of V_{dd} and sensitivity is calculated at different value of threshold voltages. Delay and power are also calculated for decoder. We have done comparison between chip circuits both containing chip bank and without chip bank and find that containing chip bank has less power dissipation in comparison to the chip architecture without chip bank. From all these analysis we have find that:

1. Power increases by increasing voltages and temperature.
2. Delay reduces by increasing voltages.
3. CMRR increases by increasing voltages.
4. Power is reduced by using bank partitioning method.

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